EQP200-LR4

Single-Mode 200G QSFP56 10km Transceiver

PRODUCT FEATURES

- **Supports 212.5Gbps**
- **Single 3.3V Power Supply**
- **Power dissipation < 6.0W**
- **Up to 10km over SMF**
- **4x26.5625GBd (PAM4) electrical interface**
- **LC connector**
- **Relaxed commercial case temperature range of 0°C to 70°C**
- **Cooled DML LAN-WDM transmitter**
- **PIN and TIA array on the receiver side**
- **I2C interface with integrated Digital Diagnostic Monitoring**
- **Safety Certification: TUV/UL/FDA**

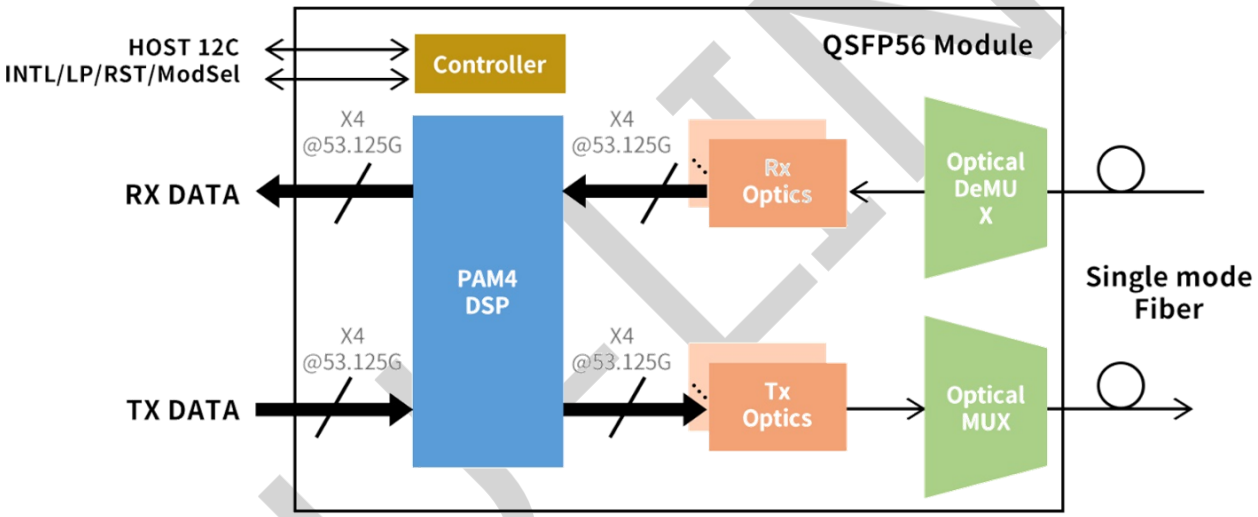
APPLICATIONS

- **200G QSFP56 10km applications with or without FEC**

DESCRIPTIONS

The ETU-Link's QSFP56 transceiver is designed for use in 200 Gigabit Ethernet links over 10km single mode fiber. The module has 4 independent electrical input/output channels operating at 26.5625GBd per channel. This transceiver consist a transmitter/receiver unit operating on a set of 4 wavelengths on the LAN-WDM group near 1300nm. The transmitter path of the module incorporates a bi-directional PAM4 retimer ASIC integrated with a 4-channel modulator driver, 4 externally modulated lasers and one optical multiplexer. On the receiver path, one optical de-multiplexer is coupled to 4 photodiodes and one 4-channel linear TIA arrays, along with the PAM4 re-timer. The electrical interface of the module is compliant with the 200GAUI-4 interface as defined by IEEE 802.3bs.

Module Block Diagram



Ordering Information

Part No.	Data Rate(optical)	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI
EQP200-LR4	212.5Gbps	EML	SMF	10KM	LC	0~+70°C	Y

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Receiver Damage Threshold (per Lane)	Rxdmg	5.0		dBm

Note:

1. Exceeding any one of these values may damage the device permanently.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	Tc	0		70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Operating Relative Humidity	RH	5		65	%
Power Dissipation	P_D			6.0	W

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter						
Differential data input swing per lane				900	mV_{p-p}	
Differential Input Impedance	Zin	90	100	110	Ohm	
DC common mode voltage		-350		2850	mv	
Receiver						
Differential output amplitude				900	mV_{p-p}	
Differential Output Impedance	Zout	90	100	110	ohm	
AC Common Mode Voltage				17.5	mV_{rms}	
Output Rise/Fall Time	t_r/t_f	9.5			ps	20%~80%
Eye width		0.265			UI	@TP4, all 3 PAM4 eyes, 1E-5
Eye height differential		70			mV	@TP4, all 3 PAM4 eyes, 1E-5

Optical and Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Transmitter						
Signaling Speed per Lane			26.5625±100ppm		GBd	
Modulation Format			PAM4			
Lane_1 Wavelength	λ_{C1}	1294.53	1295.56	1296.59	nm	
Lane_2 Wavelength	λ_{C2}	1299.02	1300.05	1301.09	nm	
Lane_3 Wavelength	λ_{C3}	1303.54	1304.58	1305.63	nm	

Lane_4 Wavelength	λ_{C4}	1308.09	1309.14	1310.19	nm	
Side-mode Suppression Ratio	SMSR	30			dB	
Total average launch power				11.3	dBm	
Average launch power, each lane		-3.4		5.3	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each lane		-0.4		5.1	dBm	
Difference in launch power between any two lanes (OMA_{outer})				4	dB	
Launch power in OMAouter minus TDECQ, each lane: for extinction ratio ≥ 4.5 dB for extinction ratio < 4.5 dB		 -1.8 -1.7			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	TDECQ			3.2	dB	
TDECQ-10log$_{10}$(C_{eq})				3.2	dB	
Average launch power of OFF transmitter each lane	P_off			-30	dBm	
Extinction Ratio	ER	3.5			dB	
$RIN_{15.6}OMA$	RIN			-132	dB/Hz	
Optical return loss tolerance				15.6	dB	
Transmitter reflectance				-26	dB	2
Receiver						
Signaling Speed per Lane			26.5625±100ppm		GBd	
Lane_1 Wavelength	λ_{C1}	1294.53	1295.56	1296.59	nm	
Lane_2 Wavelength	λ_{C2}	1299.02	1300.05	1301.09	nm	
Lane_3 Wavelength	λ_{C3}	1303.54	1304.58	1305.63	nm	
Lane_4 Wavelength	λ_{C4}	1308.09	1309.14	1310.19	nm	
Damage threshold each lane		6.3			dBm	
Average receive power, each lane		-9.7		5.3	dBm	
Receive power (OMA_{outer}), each lane				5.1	dBm	
Difference in receive power between any two lanes (OMA_{outer})				4.2	dB	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMA_{outer}), each lane	Sen			-7.2	dBm	

Stressed receiver sensitivity (OMA_{outer}),each lane				-5.4	dBm	
Conditions of stressed receiver sensitivity test:						3
Stressed eye closure for PAM4 (SECQ),lane under test			3.2		dB	
SECQ - $10log_{10}(Ceq)$			3.2		dB	4
OMA_{outer} of each aggressor lane			-1.2		dBm	
LOS assert	LOSA	-17			dBm	
LOS deassert	LOSD			-12	dBm	
LOS Hysteresis		0.5			dB	

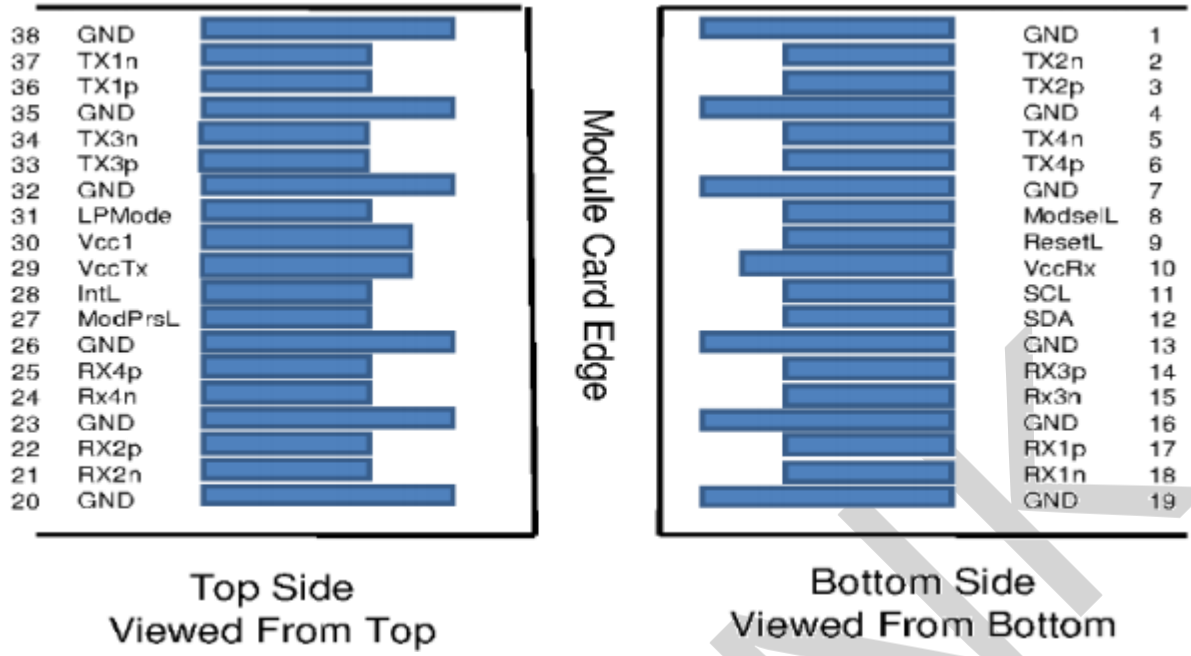
Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter.
3. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
4. Ceq is a coefficient defined in IEEE Std 802.3bs-2017 clause 121.8.5.3, which accounts for the reference equalizer noise enhancement.

Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to VCC	3%	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-3.4 to +5.3	±3	dB	Internal
Rx Receive Power (Each Lane)	-9.7 to +5.3	±3	dB	Internal

Pin Diagram



Pin Definitions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	

18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOSL	Interrupt.Optionally configurable as RxLOSL via the management interface(SFF-8636)	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode. Optionally configurable as TxDis via the management interface(SFF-8636)	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note:

1. GND is the symbol for signal and supply (power) common for the QSFP56 module. All are common within the QSFP56 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP56 Module in any combination.

Recommended Interface Circuit

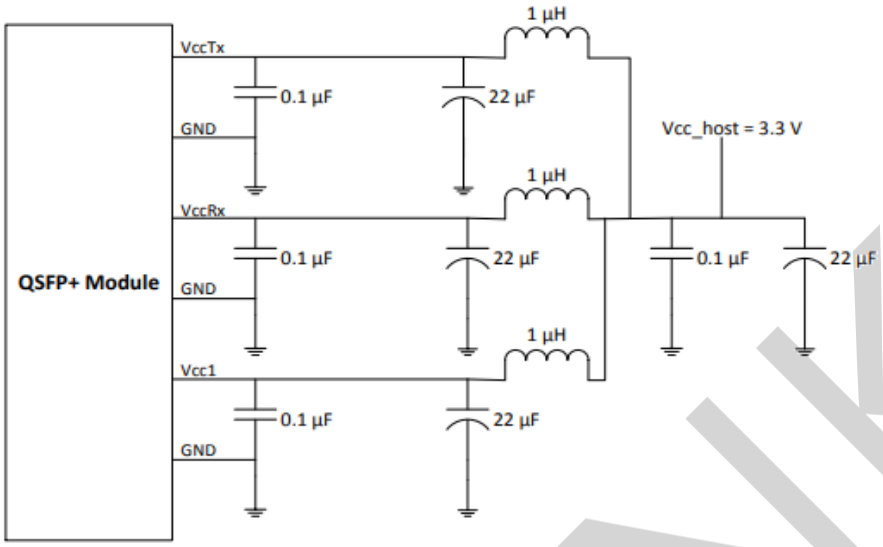
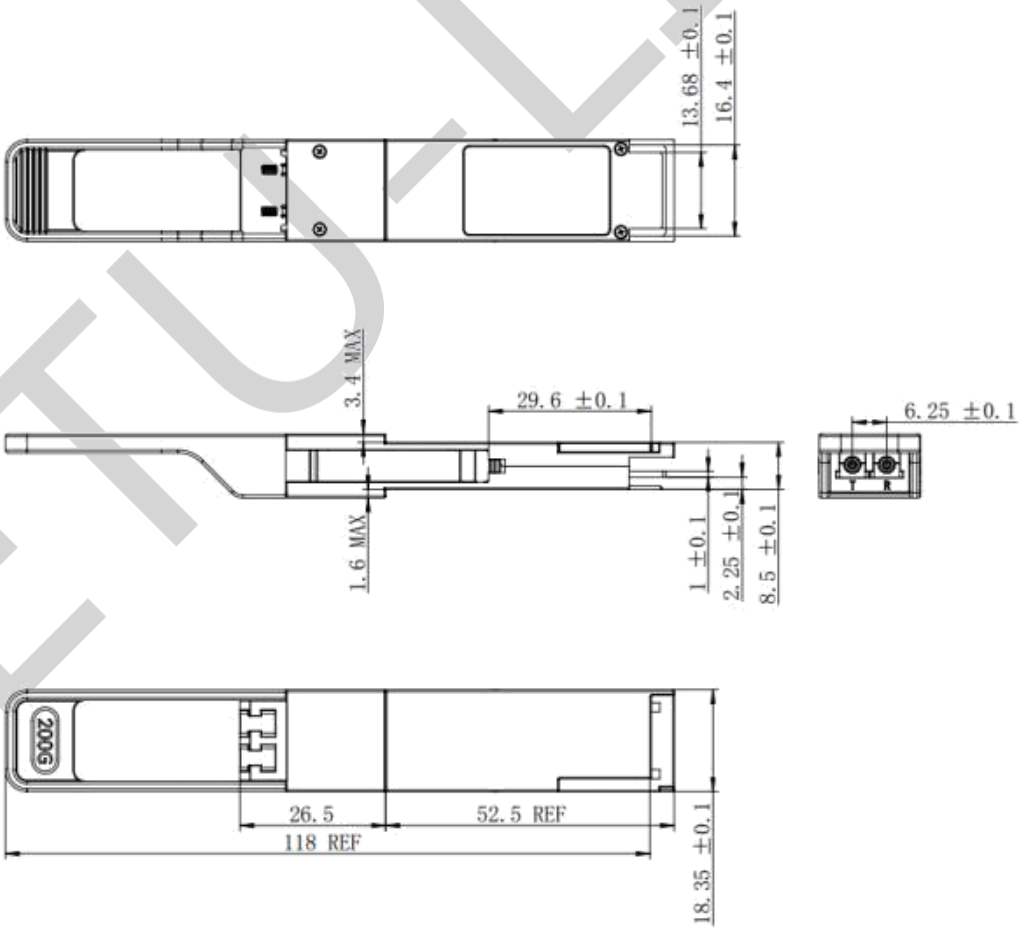


FIGURE 5-4 RECOMMENDED HOST BOARD POWER SUPPLY FILTERING

Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	February 18, 2021	Preliminary datasheet
2.1	July 17,2024	Format change

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