

## **EQD400-PLR4**

### **400G QSFP-DD PLR4 Transceiver 10KM Optical Transceiver**

#### **PRODUCT FEATURES**

- **QSFP-DD MSA compliant**
- **8x53.125Gb/s PAM4 electrical interface (400GAUI-8)**
- **SiPh based Tx with 1310 nm DFB lasers**
- **Maximum power consumption 8W**
- **4\*100 Gb/s PAM4 optic, MPO-12 APC connector**
- **Up to 10Km transmission on single mode fiber**
- **Operating case temperature: 0℃~70℃**
- **Single 3.3V power supply**
- **RoHS-6 compliant**

#### **APPLICATIONS**

- **400G Ethernet**
- **Data Center Applications**

#### **Compliance**

- **QSFP-DD MSA Rev5.1**
- **IEEE 802.3bs, IEEE 802.3cu**
- **CMIS Rev4.0**
- **RoHS compliance**
- **GR-468-CORE**

## DESCRIPTIONS

ETU-link Transceiver is a high-performance, cost-effective module for optical data communication applications supporting 400G Ethernet. The ETU-link is designed to operate in switch and router applications supporting QSFP-DD MSA / 4\*100G LR1 compliant traffic for up to 10Km links.

The ETU-link can convert 8-channel 53.125Gb/s electrical data to 4-channel 106.25Gb/s optical signals. Similarly, it optically converts 4-channel 106.25Gb/s optical signals to 8-channel electrical data output on the receiver side. It has been designed to withstand the maximum range of external operating conditions including temperature, humidity and EMI. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

## Ordering Information

Part No.	Data Rate(optical)	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI	Latch Color
EQD400-PLR4	400Gbps	DFB	SMF	10km	LC	0~70°C	Yes	Blue

## Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	TSTG	-40		85	°C	
Operating Relative Humidity	RH	5		85	%	Note1
Supply Voltage	VCC	-0.5	3.3	3.6	V	
Damage Threshold, each lane		5			dBm	

Note:

[1] Non-condensing.

## Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Case temperature	Tcase	0		70	°C	
Supply Voltage	VCC	3.135	3.3	3.465	V	
Supply Current	ICC			2552	mA	
Module Power Dissipation	P			8	W	

## Optical , Electrical Characteristic

Parameter	Symbol	Min	Typical	Max	Units	Notes
Optical Data Rate, each Lane		53.125±100ppm			GBd	
Modulation Format		PAM4				
Line wavelengths	$\lambda$	1304.5	1311	1317.5	nm	
Average Launch Power, each lane	P <sub>AVG</sub>	-1.9		4.8	dBm	
Optical Modulation Amplitude (OMA), each lane for TDECQ < 1.4 dB for 1.4 dB < TDECQ < 3.4 dB	OMA	1.1 -0.3+TDECQ		5	dBm	
Extinction Ratio	ER	3.5			dB	
Side-Mode Suppression Ratio	SMSR	30			dB	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ			3.4	dB	
Transmitter eye closure for PAM4 (TECQ)	TECQ			3.4	dB	
TDECQ - TECQ				2.5	dB	
Over/under-shoot				22	%	
Transmitter power excursion				2.8	dB	

Optical Return Loss Tolerance	dB			15.6	dB	
Transmitter Reflectance				-26	dB	
Average Launch Power of OFF Transmitter, each Lane				-15	dBm	
RIN OMA				-136	dB/Hz	

**Receiver Operating Characteristic-Optical , Electrical**

Parameter	Symbol	Min	Typical	Max	Units	Notes
Optical Data Rate, each Lane		53.125±100ppm			GBd	
Modulation Format		PAM4				
Damage threshold	PIN	5.8			dBm	1
Line wavelengths	$\lambda$	1304.5	1311	1317.5	nm	
Average receiver power, each lane		-8.2		4.8	dBm	
Receiver power, each lane (OMA)				5	dBm	
Receiver Sensitivity (OMA <sub>outer</sub> ) , each lane for TECQ < 1.4 dB for 1.4 dB < TECQ < 3.4 dB				-6.1 -7.5 + TECQ	dBm	
Stressed receiver sensitivity (OMA <sub>outer</sub> ), each lanned (max)	SRS			-4.1	dBm	2
LOSA		-15			dBm	
LOSD				-9	dBm	
LOSH		0.5			dB	
Receiver reflectance				-26	dB	
Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4				3.4	dB	

SECQ-10*Ig(Ceq)				3.4	dB	
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Note:

[1] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.

[2] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

## Digital Diagnostic Functions

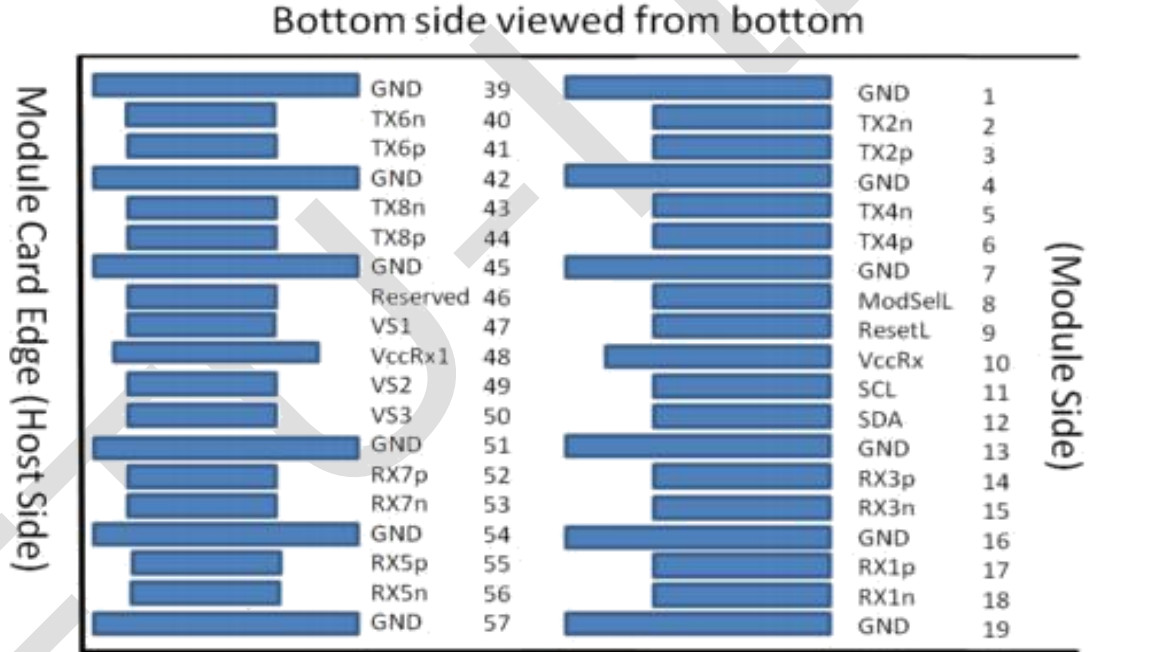
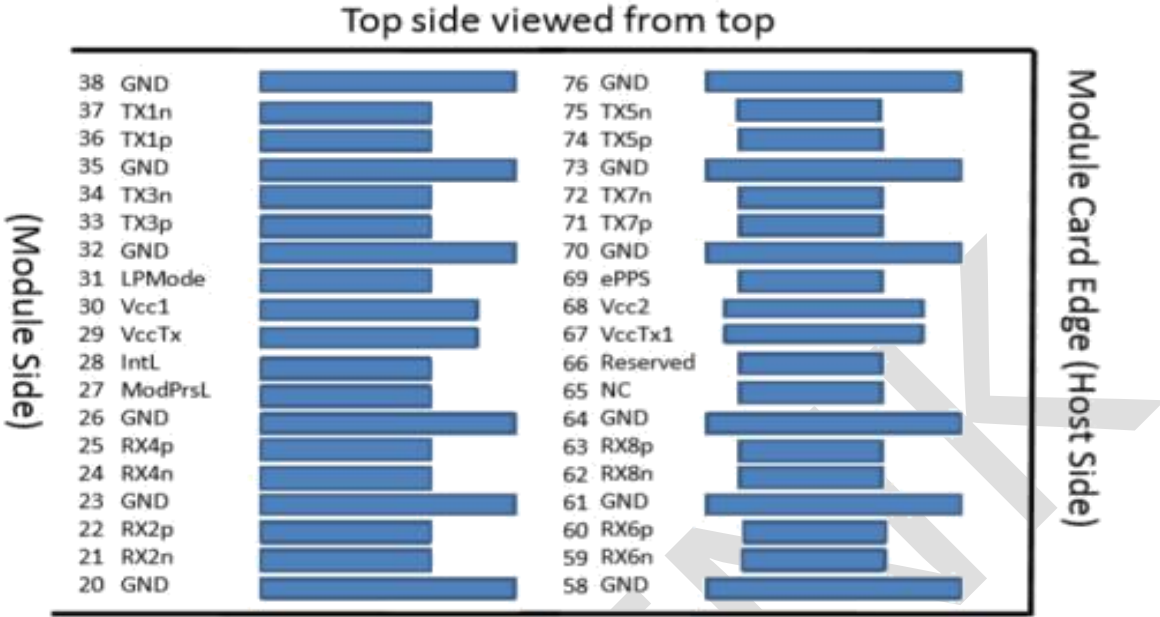
Parameter	Symbol	Min	Typical	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3		3	°C	Note1
Supply voltage monitor absolute error	DMI_Vcc	-3%		3%	V	Note2
Bias current monitor absolute error	DMI_Ibias	-10%		10%	mA	
Laser power monitor absolute error	DMI_Tx	-3		3	dB	
RX power monitor absolute error	DMI_Rx	-3		3	dB	

Notes:

[1] Temperature here is depending on module case around Max power dissipation. Temperature monitor is done over operating temperature.

[2] Supply voltage monitor is done over operating voltage.

# Pin-out Definitions



## Pin Definitions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	Note1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	Note1
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	Note1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		Vcc Rx	+3.3V Power Supply Receiver	2B	Note2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	Note1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	Note1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	Note1
20		GND	Ground	1B	Note1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	Note1
24	CML-O	Rx4n	Receiver Non-Inverted Data Output	3B	

25	CML-O	Rx4p	Receiver Inverted Data Output	3B	
26		GND	Ground	1B	Note1
27	LVTTL-I	ModPrsL	Module Present	3B	
28	LVTTL-I	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	Note2
30		Vcc1	+3.3V Power supply	2B	Note2
31	LVTTL-I	LPMODE	Low Power Mode	3B	
32		GND	Ground	1B	Note1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	Note1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	Note1
39		GND	Ground	1A	Note1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	Note1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	Note1
46		Reserved	For future use	3A	Note3
47		VS1	Module Vendor Specific 1	3A	Note3
48		VccRx1	+3.3V Power supply	2A	Note2
49		VS2	Module Vendor Specific 2	3A	Note3
50		VS3	Module Vendor Specific 3	3A	Note3
51		GND	Ground	1A	Note1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	

53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	Note1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	Note1
58		GND	Ground	1A	Note1
59	CML-O	Rx6n	Receiver Non-Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Inverted Data Output	3A	
61		GND	Ground	1A	Note1
62	CML-O	Rx8n	Receiver Non-Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Inverted Data Output	3A	
64		GND	Ground	1A	Note1
65		NC	No Connect	3A	Note3
66		Reserved	For Future Use	3A	Note3
67		VccTx1	+3.3V Power supply	2A	Note2
68		Vcc2	+3.3V Power supply	2A	Note2
69	LVTTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	Note3
70		GND	Ground	1A	Note1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	Note1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	Note1

Notes:

[1] QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect

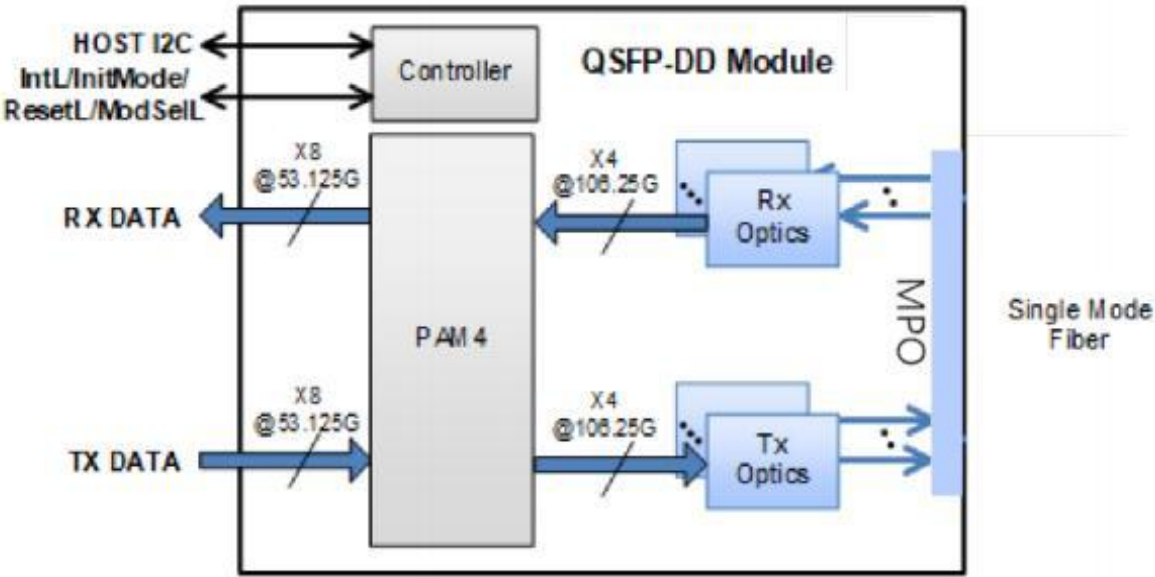
these directly to the host board signal-common ground plane.

[2] VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6 from QSFP-DD MSA. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

[3] All Vendor Specific, Reserved and No Connect and ePPS(if not used) pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

[4] Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A,2A,3A,1B,2B,3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.

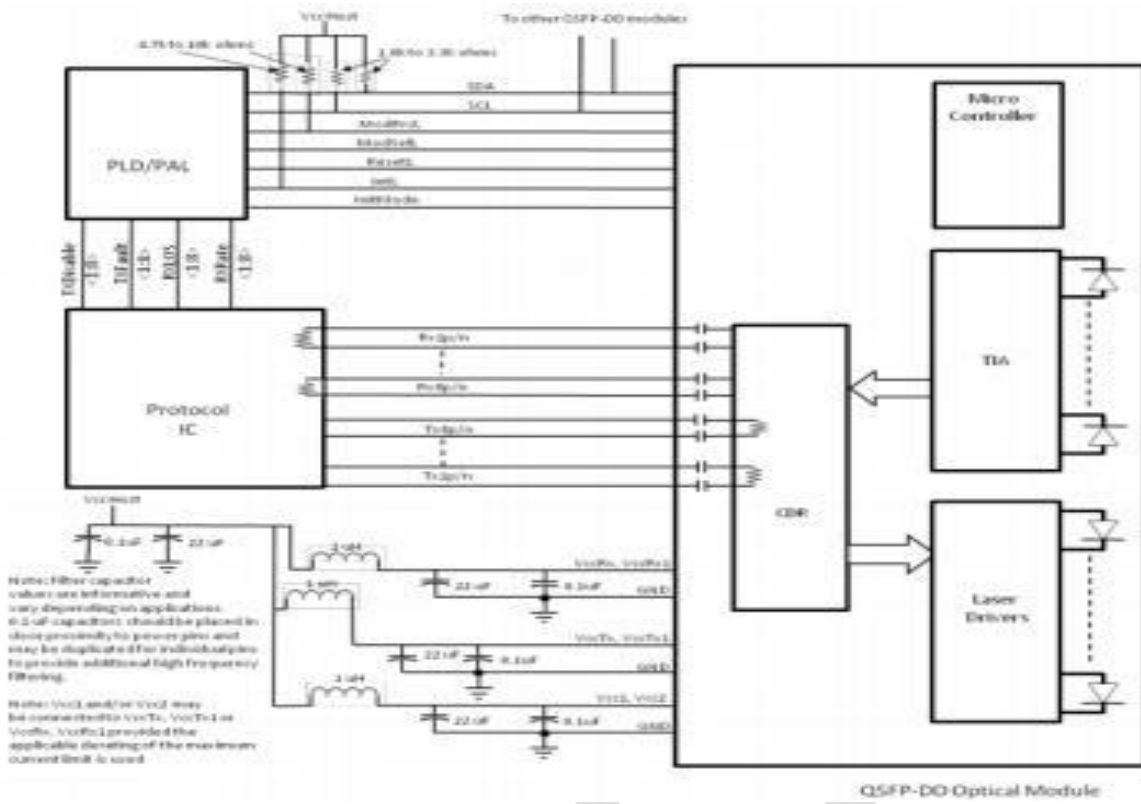
### Block Diagram of Transceiver



<Transmitter Section>: The MQD-35F2C-3 converts 8-channel 53.125Gb/s electrical data to 4-channel 1310nm 106.25Gb/s optical signals for 425Gb/s optical transmission.

<Receiver Section>: Similarly, it optically converts 4-channel 1310nm 106.25Gb/s optical signals to 8-channel electrical data output on the receiver side.

### Recommended Interface Circuit



### Mechanical Diagram

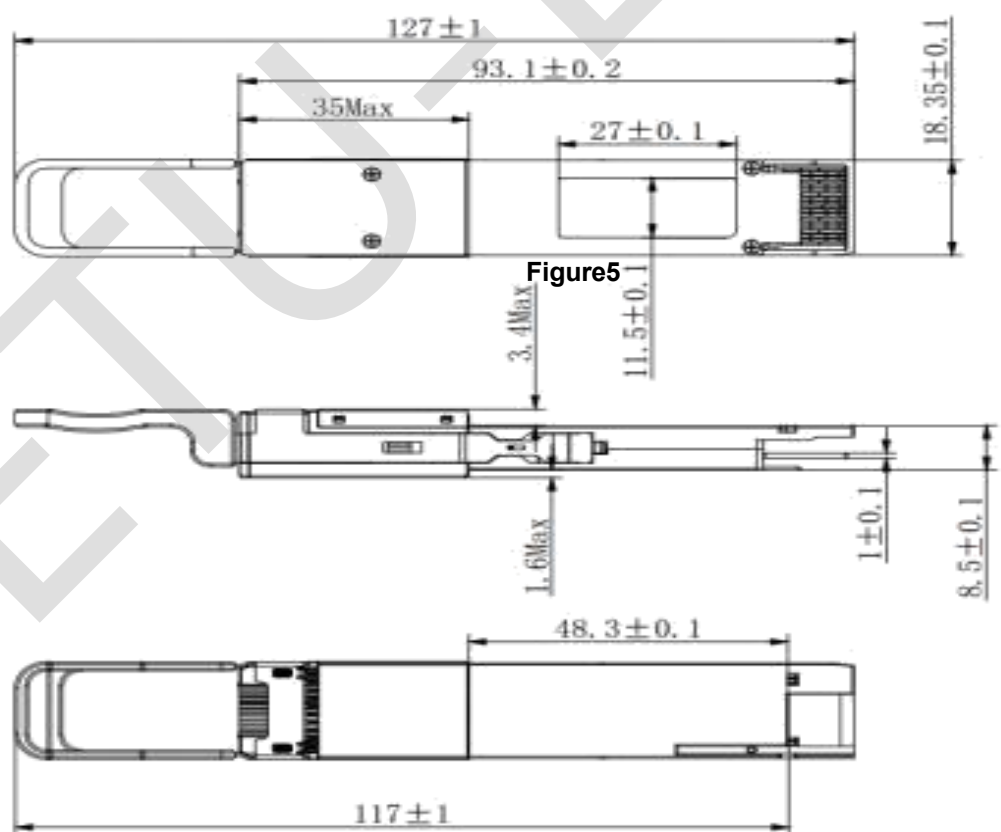


Figure5

## Revision History

Version No.	Date	Description
1.0	Aug 18, 2024	Preliminary datasheet

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