EQD400-FR4-2

400G QSFP-DD FR4 2km SMF Duplex LC EML Optical transceiver

PRODUCT FEATURES

- **Supports 425Gbps**
- **Single 3.3V Power Supply**
- **Power Dissipation < 10W**
- **Up to 2km over SMF**
- **RoHS Compliant**
- **QSFP-DD MSA Compliant**
- **8x53.125Gbps (PAM4) Electrical Interface**
- **Duplex LC Connector**
- **Commercial Case Temperature Range of 0°C to 70°C**
- **PIN and TIA Array on the Receiver Side**
- **I2C Interface with Integrated Digital Diagnostic Monitoring**
- **Driver and TIA integrated in the DSP at transmitter and receiver side**

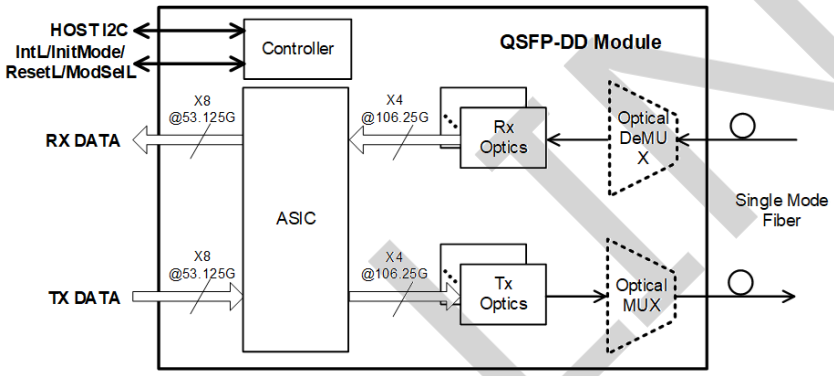
APPLICATIONS

- **Data Center**
- **Ethernet**

DESCRIPTIONS

ETU-Link's QSFP-DD 400Gbps optical module designed for 2km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals and multiplexes them into a single channel for 400Gb/s optical transmission. On the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals and converts them to 8 channels of 50Gb/s (PAM4) electrical output data. The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. Host FEC is required to support up to 2km fiber transmission.

Module Block Diagram



Ordering Information

Part No.	Data Rate(optical)	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI
EQD400-FR4-2	425Gbps	EML	SMF	2km	Duplex LC	0~70°C	Y

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	Ts	-40		+85	°C
Transceiver Power Consumption				10	W
Transceiver Power Supply Total Current				2550	mA
AC Coupling Internal Capacitor			0.1		uF
Supply Voltage	VCC	-0.5	3.3	+3.6	V
Operating Relative Humidity	RH	5		85	%
Data Input Voltage(Single Ended)		-0.5		VCC+0.5	V

Data Input Voltage(Differential)				0.8	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	TC	0		70	°C
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Power Supply Noise				66	mVpp
Power Dissipation	PD			10	W
Electrical Signal Rate Per Channel			26.5625		GBd
Optical Signal Rate Per Channel			53.125		GBd
Receiver Differential Data Output Load			100		Ohm
Fiber Length				2000	m

High Speed Electrical Input Characteristics

Parameter	Min.	Typical	Max.	Unit	Conditions
Signaling Rate Per Lane		26.5625		GBd	+/- 100 ppm
Differential peak-peak Input Voltage Tolerance	900			mV	
Differential input Return Loss(min)		Equation (83E-5)		dB	802.3bs
Differential to common mode input return loss (min)		Equation (83E-5)		dB	802.3bs
Differential Termination Mismatch			10	%	
Single-ended voltage tolerance range	-0.4		3.3	v	
DC common-mode output voltage	-350		2850	mV	
Eye width		0.22		UI	
Applied peak-peak sinusoidal jitter		Table 120E-6			802.3bs

High Speed Electrical Output Characteristics

Parameter	Min.	Typical	Max.	Unit
Signaling Rate Per Lane (Range)		26.5625 ± 100 ppm		GBd

Common Mode Voltage	-350		2850	mV
Differential pk-pk Input Voltage Tolerance			900	mV
Differential input Return Loss(min)		Equation (83E-5)		dB
Differential to common mode input return loss (min)		Equation (83E-5)		dB
Differential Termination Mismatch			10	%
Transition time (20% to 80%)	9.5			ps

High Speed Optical Transmitter Characteristics@TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling Speed per Lane			106.25		Gbps
Modulation Format			PAM4		
Lane_0 Center Wavelength	λC0	1264.5	1271	1277.5	nm
Lane_1 Center Wavelength	λC1	1284.5	1291	1297.5	nm
Lane_2 Center Wavelength	λC2	1304.5	1311	1317.5	nm
Lane_3 Center Wavelength	λC3	1324.5	1331	1337.5	nm
Side-Mode Suppression Ratio	SMSR	30			dB
Extinction Ratio	ER	3.5			dB
Total average launch power				9.3	dBm
Transmit Average Each Lane	TxAVG	-3.2		3.5	dBm
Transmit OMA Each Lane	TxOMA	-0.2		3.7	dBm
Difference in launch power between any two lanes (OMAouter)				4	dB
Launch Power In OMA-TDECQ For Extinction Ratio ≥ 4.5 dB For Extinction Ratio < 4.5 dB	OMAouter -TDECQ	-1.7 -1.6			dBm
Transmitter and Dispersion Eye Closure, each Lane	TDECQ			3.4	dB
TDECQ－10*Log10(Ceq)				3.4	dB
Difference in launch power between any two lanes (OMAouter)				4	dB
TDEC(PAM4)				3.4	dB
| TDECQ- TECQ |				2.5	dB

Transmitter transition time				17	ps
RIN17.1OMA				-136	dB/Hz
Average Launch Power of OFF Transmitter	Poff			-16	dBm
Optical Return Loss Tolerance				17.1	dB
Transmitter Reflectance				-26	dB
Transmitter over/under-shoot				22	%

High Speed Optical Receiver Characteristics@TP3 Test Point

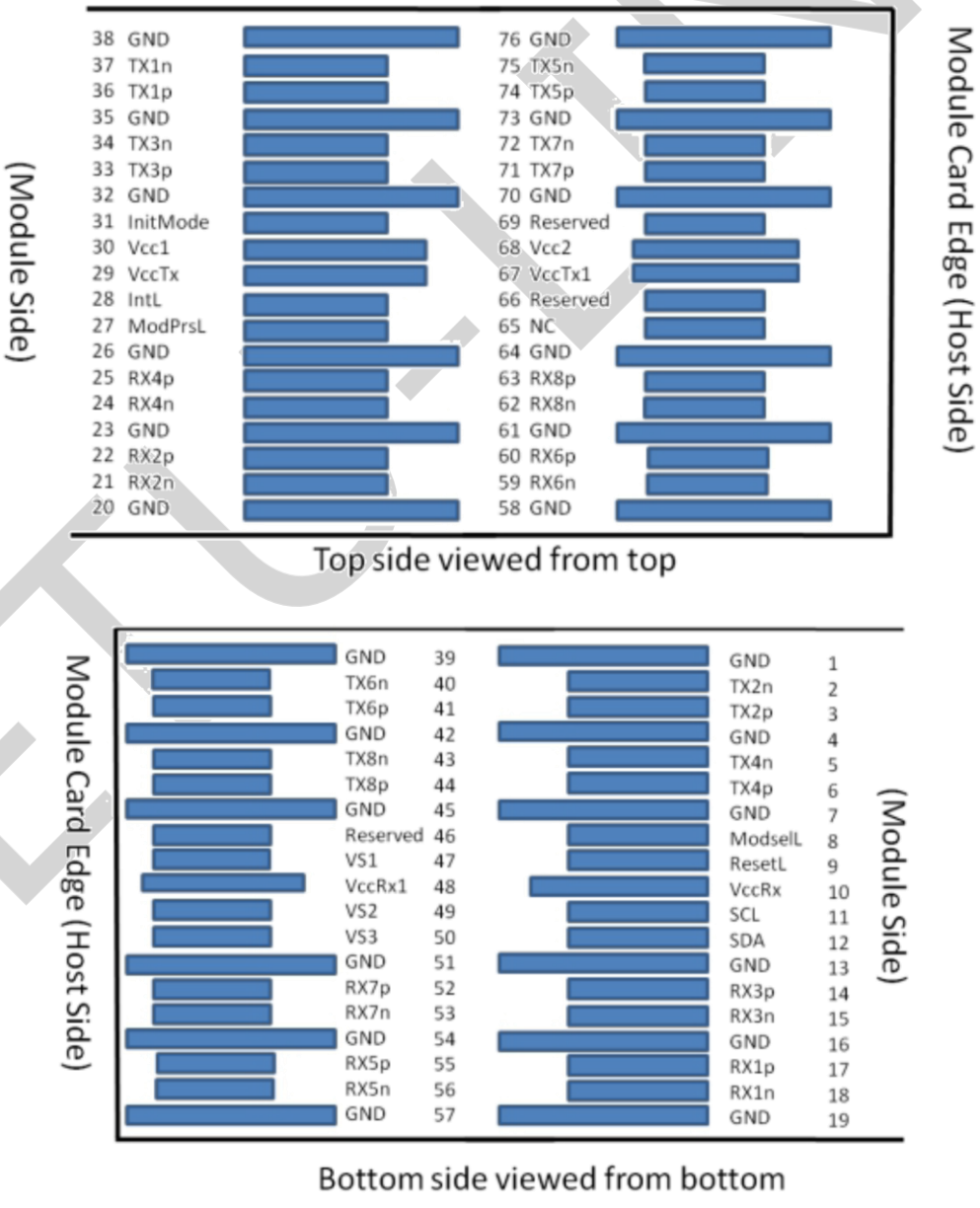
Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling Speed per Lane		106.25			Gbps
Modulation Format		PAM4			
Lane_0 Center Wavelength	λC0	1264.5	1271	1277.5	nm
Lane_1 Center Wavelength	λC1	1284.5	1291	1297.5	nm
Lane_2 Center Wavelength	λC2	1304.5	1311	1317.5	nm
Lane_3 Center Wavelength	λC3	1324.5	1331	1337.5	nm
Damage Threshold				4.5	dBm
Average Receive Power Each Lane	RxAVG	-7.2		3.5	dBm
Receive Power (OMA) Each Lane	RxOMA			3.7	dBm
Difference in receive power between any two lanes(OMAouter)				4.1	dB
Receiver sensitivity (OMAouter), each lane	SenOMA			max (-4.6, -6+TECQ)	dBm
LOS Assert	LOSA	-30		-7.5	dBm
LOS De-Assert	LOSD	-29.5		-7	dBm
Los Hysteresis		0.5			dB
RSSI accuracy		-2		+2	dB
Receiver Reflectance				-26	dB

Digital Diagnostics

Digital diagnostic management interface (DDMI) is realized by I2C interface in compliance with CMIS 4.0. diagnostic management functions are realized, and the data addresses are listed in the form below.

Performance item	Data address		
	Alarm & Warning	Alarm & Warning thresholds	Monitor
Module temperature	Lower page 9	Page2h (128-135)	Lower page (14-15)
Module voltage	Lower page 9	Page2h (136-143)	Lower page (16-17)
Bias current	Page11h (143-146)	Page2h (184-191)	Page11h (170-177)
Transmitter optical power	Page11h (139-142)	Page2h (176-183)	Page11h (154-161)
Receiver optical power	Page11h (149-152)	Page2h (192-199)	Page11h (186-193)

Pin Diagram



Pin Definitions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL /RxLOS	Interrupt/optional RxLOS	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode/ TxDIS	Low Power Mode / optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	

37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		VS4	Module Vendor Specific 4	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		ePPS/Clock	1 PPS PTP clock or reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	

76		GND	Ground	1A	1

Notes;

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1500 mA.

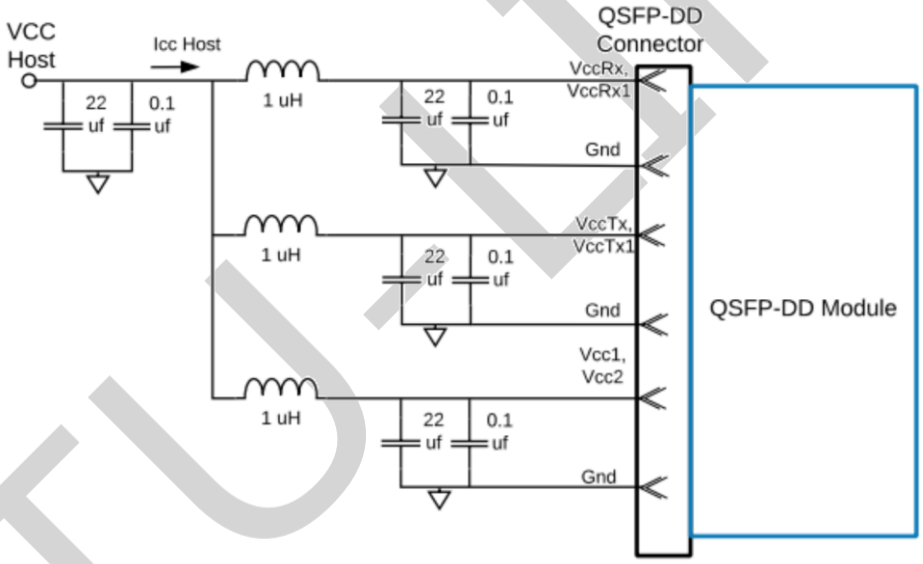
3. Reserved and No Connect pins may be terminated with 10k ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 k Ohms and less than 100 pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

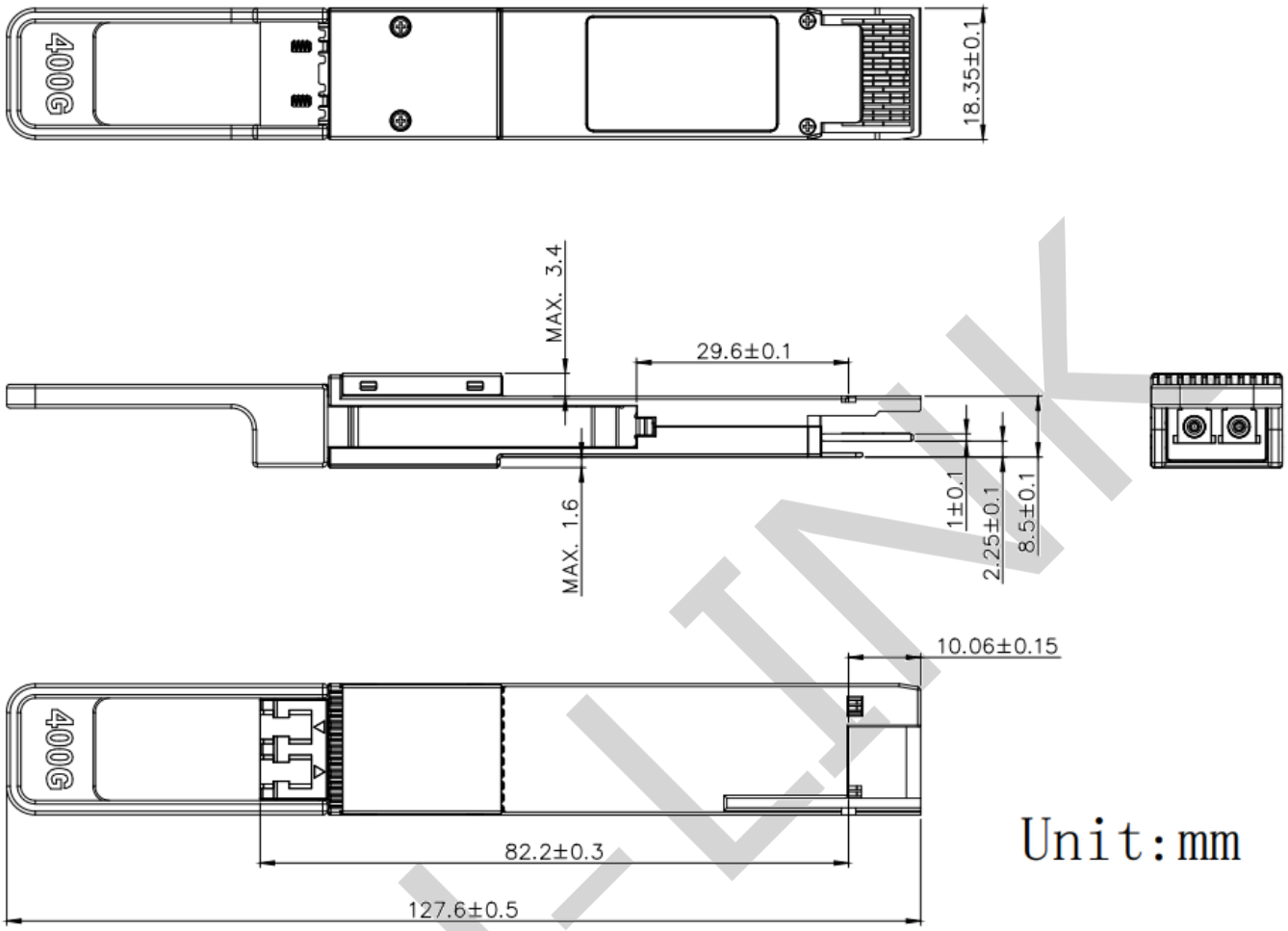
5. Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10k ohms.

6. The ePPS/Clock pin is pulled down to ground with 10km ohms on the module.

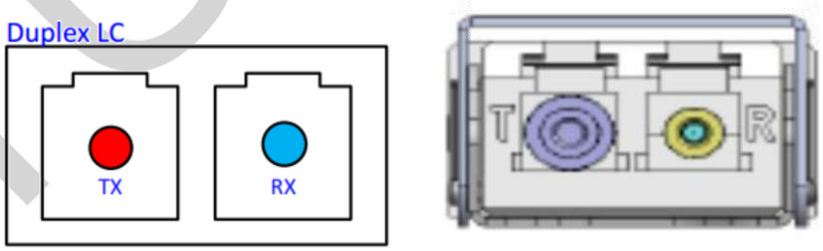
Recommended Interface Circuit



Mechanical Diagram



The optical interface port is a duplex LC connector as specified in IEC 61754-20.



Module Optical Interface (looking into the optical port)

Revision History

Version No.	Date	Description
1.0	Aug 18 2023	Preliminary datasheet
2.0	July 26, 2024	Format change

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