

EOP800-DR4-RHS

800G OSFP 2xDR4 500m SMF Dual MPO12 Optical Transceiver

PRODUCT FEATURES

- Supports 850Gbps
- Single 3.3V Power Supply
- Up to 500m over SMF with KP4 FEC
- Dual MPO-12 connector
- Power dissipation < 16W
- Sipro based transmitter
- Case temperature range: 0°C to 70°C (commercial)
- RoHS Compliant
- Safety Certification: CB/cTUVus/EU/FDA/FCC/EMC

APPLICATIONS

- Data Center
- AI

DESCRIPTIONS

ETU-LINK's OSFP transceiver module is designed for use in 800 Gigabit Ethernet links over 500m single mode fiber. The module includes eight parallel channels with a central wavelength of 1310nm, and the operating rate of each channel is 106.25Gbps. These 8-channel PAM4 parallel optical signals can be converted into 8-channel PAM4 electrical output signals; and there are 8 independent electrical input/output channels, which can convert PAM4 electrical input data into 8-channel PAM4 parallel optical signal. The electrical interface of the module is compliant with the 800 GAUI-8 interface as defined by IEEE 802.3ck, and compliant with OSFP MSA.

Ordering Information

Part No.	Description
EOP800-DR4	OSFP 800G 2*DR4 Optical transceiver for flat top solution

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	TS	-40		+85	°C
Supply Voltage	VCC	-0.5	3.3	+3.6	V
Operating Relative Humidity	RH	5		95	%
Data Input Voltage Single Ended		-0.5		Vcc+0.5	V
Data Input Voltage Differential				0.8	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	TC	0		70	°C
Power Dissipation	PD			16	W
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Power Supply Noise				50	mVpp
Electrical Signal Rate Per Channel (PAM encoded)			53.125		GBd

Optical Signal Rate Per Channel (PAM encoded)			53.125		GBd
Receiver Differential Data Output Load		100			Ohm
Fiber Length (9μm SMF)				500	m

Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Conditions
Transceiver Power Consumption				16	W	
Transceiver Power Supply Total Current				5104	mA	
Ac Coupling Internal Capacitor			0.1		uF	

High Speed Electrical Input Characteristics

Parameter	Test Point	Min.	Typical	Max.	Unit	Conditions
Signaling Rate Per Lane (Range)	TP1	53.125± 100 ppm			GBd	
Differential peak-peak Input Voltage Tolerance	TP1a	750			mV	
Peak-to-peak AC common-mode voltage tolerance	TP1a				mV	
Low-frequency, VCMLF		32				
Full-band, VCMFB		80				
Differential-mode to common-mode return loss, RLcd	TP1	Equation (120G-2)			dB	802.3ck
Effective return loss, ERL	TP1	8.5			dB	
Differential Termination Mismatch	TP1			10	%	
Module stressed input Tolerance	TP1a		See 120G.3.4.3			802.3ck
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode voltage Tolerance	TP1	-350		2850	mV	
Module stressed input tolerance test						
Pattern generator transition Time			9		ps	
Applied peak-peak sinusoidal Jitter			Table 162-17			802.3ck

Eye height			10		mV	
Vertical eye closure, VEC		12		12.5	dB	
Crosstalk differential peak-to-peak voltage			845		mV	
Crosstalk transition time			8.5		ps	

High Speed Electrical Output Characteristics

Parameter	Test Point	Min.	Typical	Max.	Unit
Signaling Rate Per Lane (Range)	TP4	53.125± 100 ppm			GBd
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB	TP4			32 80	mV
Differential Peak-To-Peak Output Voltage Short mode Long mode	TP4			600 845	mV
Eye height	TP4	15			mV
Vertical eye closure, VEC	TP4			12	dB
Common-mode to differential- mode return loss, RLdc	TP4	Equation (120G-1)			dB
Effective Return Loss	TP4	8.5			dB
Differential Termination Mismatch	TP4			10	%
Transition Time	TP4	8.5			ps
DC Common Mode Voltage	TP4	-350		2850	mV

Optical and Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Signaling Speed per Lane		53.125±100ppm			GBd
Modulation Format		PAM4			
Center Wavelength	λ	1304.5	1311	1317.5	nm
Side-mode Suppression Ratio	SMSR	30			dB
Transmit Average Each Lane	TxAVG	-2.9		4	dBm

Outer Optical Modulation Amplitude (OMA _{outer}), each lane	TxOMA	0.8	-	4.2	dBm
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.4	dB
Launch Power in OMA _{outer} -TDECQ		-2.2			dBm
Average launch power of OFF transmitter, each lane				-15	dBm
Extinction Ratio	ER	3.5			dB
RIN17.1 OMA				-136	dB/Hz
Optical Return Loss Tolerance				21.4	dB
Transmitter Reflectance				-26	dB
Receiver					
Signaling Speed per Lane		53.125±100ppm			GBd
Modulation Format		PAM4			
Center Wavelength	λ	1305.5	1311	1317.5	nm
Damage threshold, each lane		5			dBm
Average receiver power each lane	RxAVG	-5.9		4	dBm
Receive power (OMA _{outer}) each Lane	RxOMA			4.2	dBm
Receiver Reflectance				-26	dB
Receiver sensitivity (OMA _{outer}) each Lane	Sen			-3.9	dBm
RSSI accuracy		-3		+3	dB
LOS Assert	LOSA	-30		-7.5	dBm
LOS De-Assert	LOSD	-29.5		-7	dBm
LOS Hysteresis		0.5			dB

Pin Diagram



Pin Definitions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
3	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
6	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
7		GND	Ground	1B	1
8	CML-I	Tx6p	Transmitter Data Non-Inverted	3B	
9	CML-I	Tx6n	Transmitter Data Inverted	3B	
10		GND	Ground	1B	1
11	CML-I	Tx8p	Transmitter Data Non-Inverted	3B	
12	CML-I	Tx8n	Transmitter Data Inverted	3B	
13		GND	Ground	1B	1

14	LVCMS-I/O	SCL	2-wire Serial interface clock	3B	2
15		VCC	+3.3V Power	2B	
16		VCC	+3.3V Power	2B	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present	3B	
18		GND	Ground	1B	1
19	CML-O	Rx7n	Receiver Data Inverted	3B	
20	CML-O	Rx7p	Receiver Data Non-Inverted	3B	
21		GND	Ground	1B	
22	CML-O	Rx5n	Receiver Data Inverted	3B	
23	CML-O	Rx5p	Receiver Data Non-Inverted	3B	
24		GND	Ground	1B	1
25	CML-O	Rx3n	Receiver Data Inverted	3B	
26	CML-O	Rx3p	Receiver Data Non-Inverted	3B	
27		GND	Ground	1B	1
28	CML-O	Rx1n	Receiver Data Inverted	3B	
29	CML-O	Rx1p	Receiver Data Non-Inverted	3B	
30		GND	Ground	1B	1
31		GND	Ground	1B	1
32	CML-O	Rx2p	Receiver Data Non-Inverted	3B	
33	CML-O	Rx2n	Receiver Data Inverted	3B	
34		GND	Ground	1B	1
35	CML-O	Rx4p	Receiver Data Non-Inverted	3B	1
36	CML-O	Rx4n	Receiver Data Inverted	3B	
37		GND	Ground	1B	1
38	CML-O	Rx6p	Receiver Data Non-Inverted	3B	
39	CML-O	Rx6n	Receiver Data Inverted	3B	
40		GND	Ground	1B	1
41	CML-O	Rx8p	Receiver Data Non-Inverted	3B	
42	CML-O	Rx8n	Receiver Data Inverted	3B	
43		GND	Ground	1B	1
44	Multi-Level	INT/RSTn	Module input/Module Reset	3B	
45		VCC	+3.3V Power	2B	
46		VCC	+3.3V Power	2B	
47	LVCMS-I/O	SCL	2-wire Serial interface Data	3B	2
48		GND	Ground	1B	1
49	CML-I	Tx7n	Transmitter Data Inverted	3B	
50	CML-I	Tx7p	Transmitter Data Non-Inverted	3B	
51		GND	Ground	1B	1
52	CML-I	Tx5n	Transmitter Data Inverted	3B	

53	CML-I	Tx5p	Transmitter Data Non-Inverted	3B	
54		GND	Ground	1B	1
55	CML-I	Tx3n	Transmitter Data Inverted	3B	
56	CML-I	Tx3p	Transmitter Data Non-Inverted	3B	
57		GND	Ground	1B	1
58	CML-I	Tx1n	Transmitter Data Inverted	3B	
59	CML-I	Tx1p	Transmitter Data Non-Inverted	3B	
60		GND	Ground	1B	1

Note: 1: OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise noted.

2: Open-Drain with pull up resistor on Host.

Recommended Interface Circuit

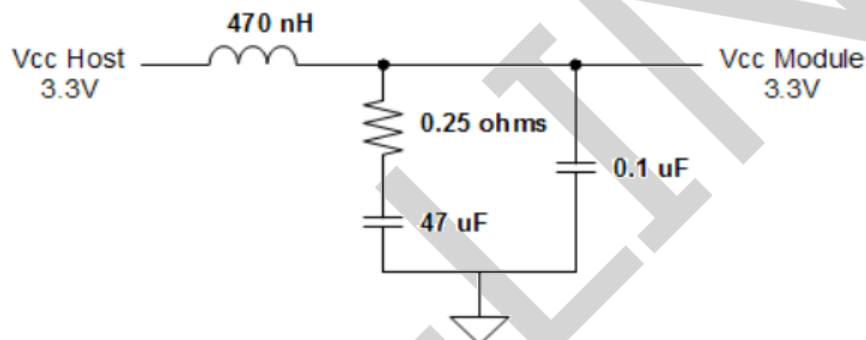
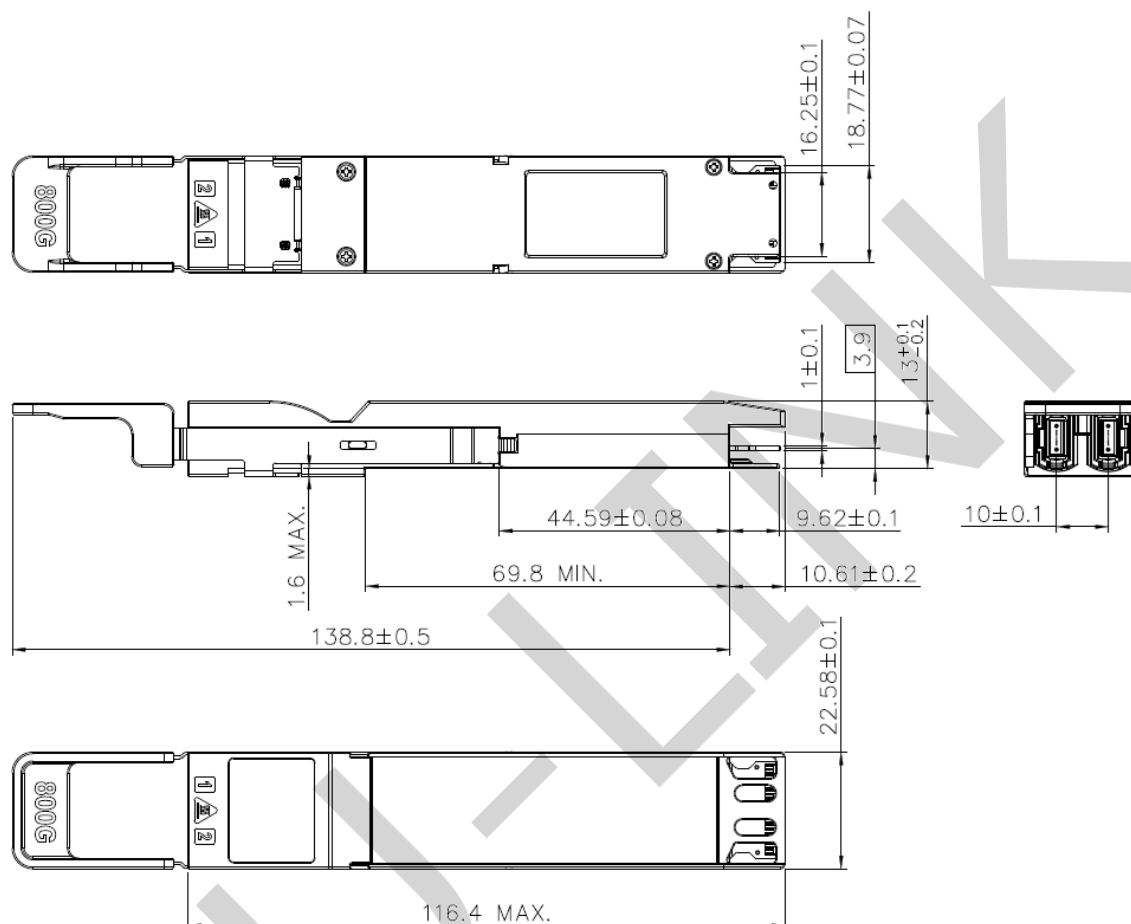


Figure 13-6: Host board power filter circuit

Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	February 12, 2025	Preliminary datasheet

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