

EDQP200-x

200Gbps QSFP56 Passive High Speed Cable (DAC)

PRODUCT FEATURES

- **Compliant with SFF-8636**
- **Compliant with IEEE802.3bj& IEEE802.3cd**
- **Support I2C two - line string interface, easy to control**
- **Support for hot plugging**
- **Low crosstalk**
- **Low power**

APPLICATIONS

- **10G/40G /100G/200G Ethernet**
- **Infiniband SDR, DDR, QDR,FDR,EDR,HDR**
- **SWITCH**
- **Router**
- **Concentrator**
- **Data center, cloud server**

Industry Standards

- **200G Ethernet(IEEE 802.3cd)**
- **InfiniBand EDR**

DESCRIPTIONS

200G QSFP56 passive cable assembly products, based on 4X25G/4X28G or 4*50G/4*56G(pam-4)/2*100Gstructure, this product can well meet the next generation of 200G switches, servers, routers and other products application needs.

The QSFP56 cable assembly is optimally designed to reduce crosstalk and plug loss, providing excellent signal integrity and fully compliant with next generation Ethernet and InfiniBand standards.

Ordering Information

Part No.	Description
EDQP200-x	200G QSFP56 Direct Attach Cable - PAM4 (DAC) xM

Notes:

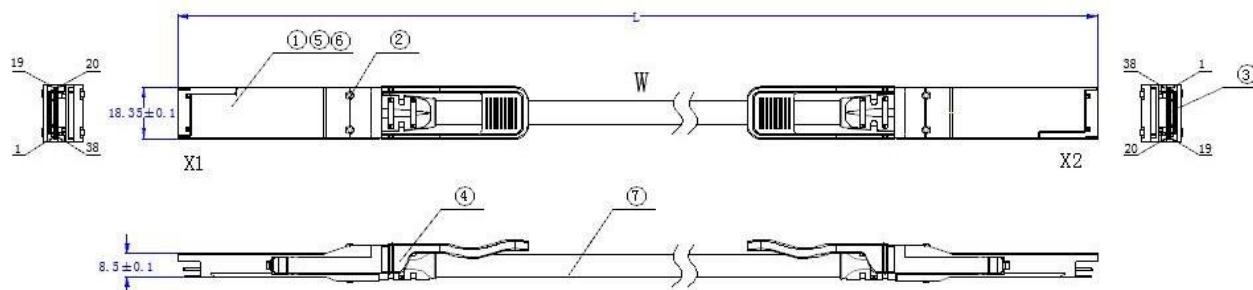
- where "x" denotes cable length in meters. Examples are as follows:
- x = 1 for 1m

Description

200G QSFP56 passive cable assembly products, based on 4X25G/4X28G or 4*50G/4*56G(pam-4)/2*100Gstructure, this product can well meet the next generation of 200G switches, servers, routers and other products application needs.

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Outline drawing



Wiring Diagram

X1	X2	REMARKS	X1	X2	REMARKS
18(RX1-)	37(TX1-)	pair	37(TX1-)	18(RX1-)	pair
17(RX1+)	36(TX1+)		36(TX1+)	17(RX1+)	
15(RX3-)	34(TX3-)	pair	34(TX3-)	15(RX3-)	pair
14(RX3+)	33(TX3+)		33(TX3+)	14(RX3+)	
6 (TX4+)	25(RX4+)	pair	25(RX4+)	6 (TX4+)	pair
5 (TX4-)	24(RX4-)		24(RX4-)	5 (TX4-)	
3 (TX2+)	22(RX2+)	pair	22(RX2+)	3 (TX2+)	pair
2 (TX2-)	21(RX2-)		21(RX2-)	2 (TX2-)	
1, 4, 7, 13, 16, 19, 20, 23, 26, 32, 35, 38	1, 4, 7, 13, 16, 19, 20, 23, 26, 32, 35, 38	GND	8, 9, 10, 11, 12, 27, 28, 29, 30, 31	8, 9, 10, 11, 12, 27, 28, 29, 30, 31	EEPROM point at both ends

Electrical Performance

1.Signal Integrity

Item		Requirement	Test Condition
Differential Impedance	Cable Impedance	105+5/-10Ω	Rise time of 25ps (20 % - 80 %).
	Paddle Card Impedance	100±10Ω	
	Cable Termination Impedance	100±15Ω	
Differential (Input/Output)Return loss S_{DD11}/S_{DD22}		$\text{Return_loss}(f) \geq \begin{matrix} 16.5-2\sqrt{f} & 0.05 \leq f < 4.1 \\ 10.66-14\log_{10}(f/5.5) & 4.1 \leq f \leq 19 \end{matrix}$ Where f is the frequency in GHz Return loss(f) is the return loss at frequency f	10MHz≤f ≤19GHz
Differential to common-mode (Input/Output)Return loss S_{CD11}/S_{CD22}		$\text{Return_loss}(f) \geq \begin{matrix} 22-(20/25.78)f & 0.01 \leq f < 12.89 \\ 15-(6/25.78)f & 12.89 \leq f \leq 19 \end{matrix}$ Where f is the frequency in GHz Return_loss(f) is the Differential to common-mode	10MHz≤f ≤19GHz

	return loss at frequency f																						
Common-mode to Common-mode (Input/Output)Return loss S_{CC11}/S_{CC22}	$Return_loss(f) \geq 2\text{dB}$ $0.2 \leq f \leq 1$ 9 Where f is the frequency in GHz $Return_loss(f)$ is the common-mode to common-mode return loss at frequency f	$10\text{MHz} \leq f \leq 19\text{GHz}$																					
Differential Insertion Loss (S_{DD21} Max.)	(Differential Insertion Loss Max. For TPa to TPb Excluding Test fixture) <table><tr><td>F AW G</td><td>1.25G Hz</td><td>2.5GHz</td><td>5.0GHz</td><td>7.0GHz</td><td>10GHz</td><td>12.89 GHz</td></tr><tr><td>30(1m)Max.</td><td>4.5dB</td><td>5.4dB</td><td>6.3dB</td><td>7.5dB</td><td>8.5dB</td><td>10.5dB</td></tr><tr><td>30/28(3m)Max</td><td>7.5dB</td><td>9.5dB</td><td>12.2dB</td><td>14.8dB</td><td>18.0dB</td><td>21.5dB</td></tr></table>	F AW G	1.25G Hz	2.5GHz	5.0GHz	7.0GHz	10GHz	12.89 GHz	30(1m)Max.	4.5dB	5.4dB	6.3dB	7.5dB	8.5dB	10.5dB	30/28(3m)Max	7.5dB	9.5dB	12.2dB	14.8dB	18.0dB	21.5dB	$10\text{MHz} \leq f \leq 19\text{GHz}$
F AW G	1.25G Hz	2.5GHz	5.0GHz	7.0GHz	10GHz	12.89 GHz																	
30(1m)Max.	4.5dB	5.4dB	6.3dB	7.5dB	8.5dB	10.5dB																	
30/28(3m)Max	7.5dB	9.5dB	12.2dB	14.8dB	18.0dB	21.5dB																	

2. Other Electrical Performance

Item	Requirement	Test Conditon
Low Level Contact Resistance	70milliohms Max. From initial.	EIA-364-23:Apply a maximum voltage of 20mV And a current of 100 mA.
Insulation Resistance	10Mohm(Min.)	EIA364-21:AC 300V 1minute
Dielectric Withstanding Voltage	NO disruptive discharge.	EIA-364-20:Apply a voltage of 300 VDC for 1minute between adjacent terminals And between adjacent terminals and ground.

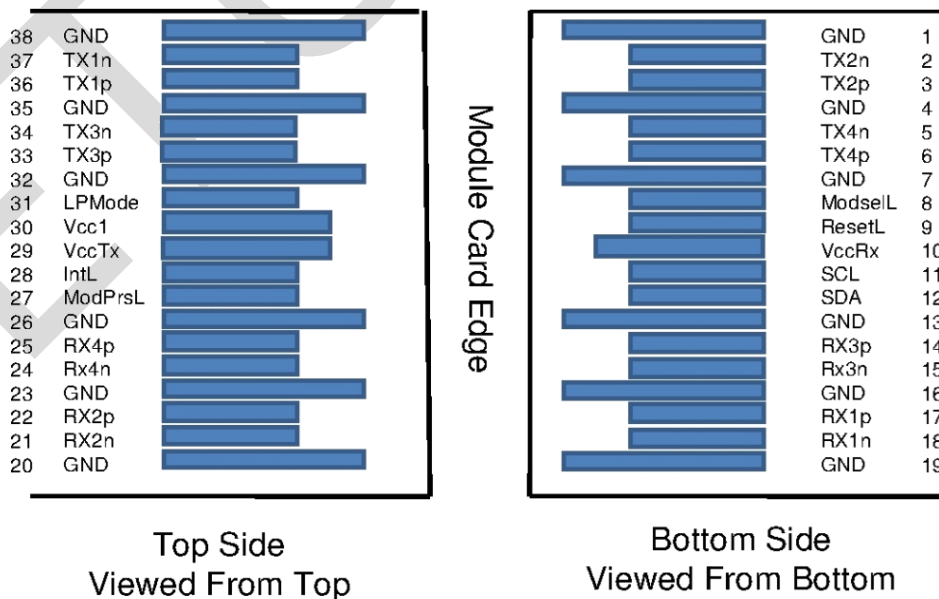
High Speed Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential Impedance	TDR	90	100	110	Ω	
Insertion loss	SDD21	-16.06			dB	At 13.28 GHz
Differential Return Loss	SDD11			See 1	dB	At 0.05 to 4.1 GHz
	SDD22			See 2	dB	At 4.1 to 19 GHz
Common-mode to common-mode output return loss	SCC11 SCC22			-2	dB	At 0.2 to 19 GHz
Differential to common-mode return loss	SCD11 SCD22			See 3	dB	At 0.01 to 12.89 GHz
				See 4		At 12.89 to 19 GHz
Differential to common Mode Conversion Loss	SCD21-IL			-10	dB	At 0.01 to 12.89 GHz
				See 5		At 12.89 to 15.7 GHz
				-6.3		At 15.7 to 19 GHz

Notes:

1. Reflection Coefficient given by equation $SDD11(dB) < -16.5 + 2 \times \text{SQRT}(f)$, with f in GHz
2. Reflection Coefficient given by equation $SDD11(dB) < -10.66 + 14 \times \log_{10}(f/5.5)$, with f in GHz
3. Reflection Coefficient given by equation $SCD11(dB) < -22 + (20/25.78)*f$, with f in GHz
4. Reflection Coefficient given by equation $SCD11(dB) < -15 + (6/25.78)*f$, with f in GHz
5. Reflection Coefficient given by equation $SCD21(dB) < -27 + (29/22)*f$, with f in GHz

Pin Diagram



Pin Descriptions

Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		Vcc Rx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	2-wire serial interface clock
12	LVC MOS-I/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt
29		Vcc Tx	+3.3V Power supply transmitter
30		Vcc1	+3.3V Power supply
31	LVTTL-I	LPMode	Low Power Mode
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground

Recommended Interface Circuit

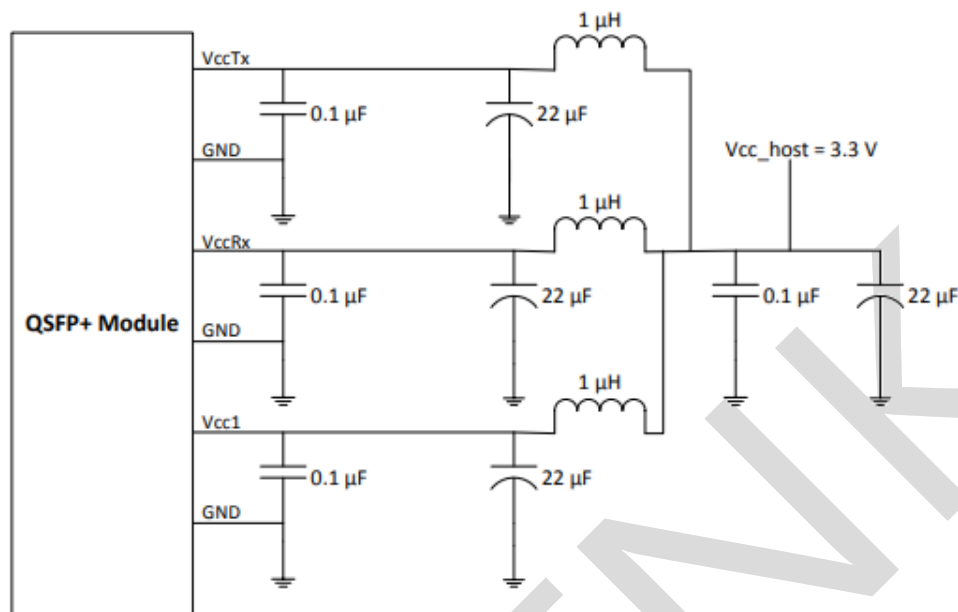
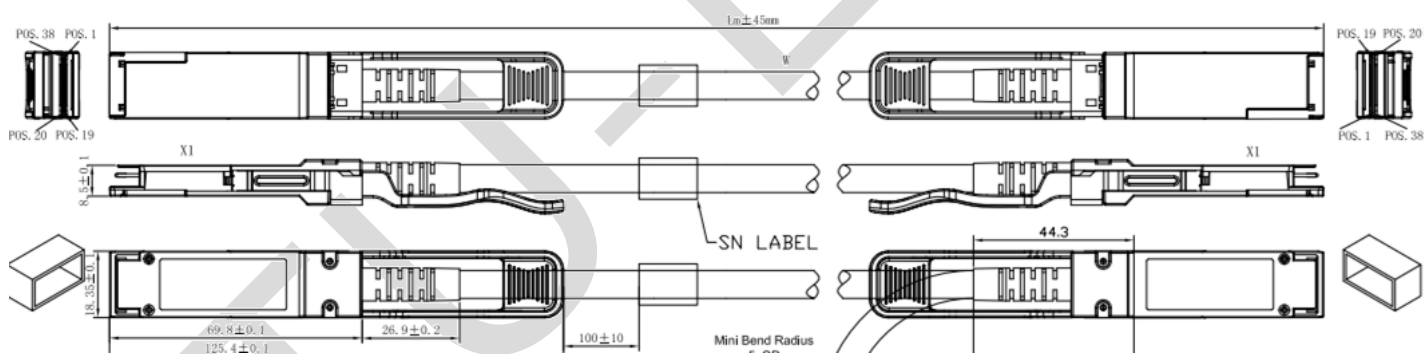


FIGURE 5-4 RECOMMENDED HOST BOARD POWER SUPPLY FILTERING

Mechanical Specifications

The connector is compatible with the SFF-8436 specification.



Length (m)	Cable AWG
1	30
2	26/30
3	26

Revision History

Version No.	Date	Description
1.0	Sep 8, 2018	Preliminary datasheet
2.0	Aug 16, 2024	Product upgrades

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