EB894X-02D

40G QSFP+ SR4 850~940nm 240m Optical Transceiver

PRODUCT FEATURES

- Compliant with QSFP+ MSA
- Compliant with SWDM MSA
- Compliant with SFF-8636
- Compliant with IEEE 802.3ba
- Hot-pluggable QSFP+ form factor
- 4x10Gb/s VCSEL-based SWDM transmitter
- Supports 41.2Gbps aggregate bit rate
- Power dissipation<3.5W
- Maximum link length of 240m on OM3 MMF and 350m on OM4 MMF
- Case temperature range of 0°C to 70°C
- Duplex LC receptacles
- XLPPI electrical interface
- RoHS compliant

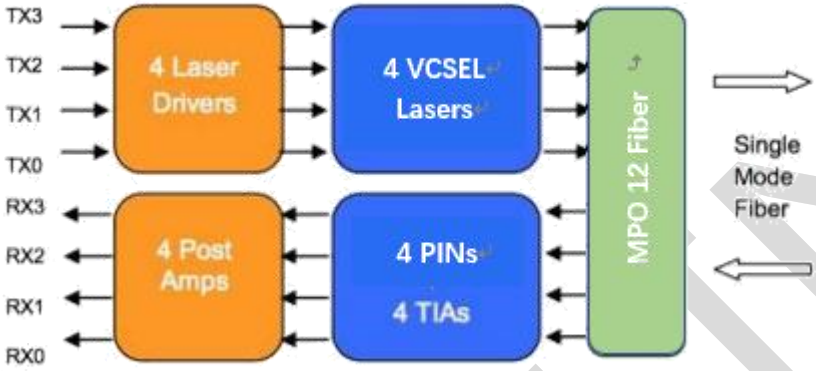
APPLICATIONS

- 40G Ethernet over Duplex MMF

DESCRIPTIONS

The 40G QSFP+ WDMS4 transceiver modules are designed for use in 40G Ethernet links over duplex multimode fiber. Four channels/lanes in the 850-940nm region @ 10Gbps to transport the Ethernet signal. Digital diagnostics functions are available via an I2C interface, as specified by the QSFP+ MSA.

Module Block Diagram



Ordering Information

Part No.	Data Rate(optical)	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI	Latch Color
EB894X-02D	41.25Gbps	Vcsel	MMF	240m	LC	0~70℃	Yes	beige

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	85	° C
Case Operating Temperature	Top	0	70	° C
Relative Humidity (non-condensation)	RH	5	95	%
Supply Voltage	Vcc	-0.5	3.6	V
Input Voltage	Vin	-0.5	VCC+0.5	V

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Top	0	70	℃
Relative Humidity(non- condensation)	RH	5	85	%
Power Supply Voltage	Vcc	3.135	3.465	V
Total Power Consumption	Pc	-	1.5	W

Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Host 2-wire Vcc voltage	Vcc_Host_2 w	3.14	3.46	V
SCL and SDA Voltage[1]	VOL	0.0	0.40	V
	VOH	Vcc_Host_2w - 0.5	Vcc_Host_2w + 0.3	V
	VIL	-0.3	VccT*0.3	V
	VIH	VccT*0.7	VccT+0.5	V
Input current on the SCL and SDA contacts	Il	-10	10	mA

Optical Characteristics

Transmitter Parameter	Lane	Min	Typical	Max	Unit	Note
Signaling rate, each lane		10.3125 , 9.953±100ppm			Gb/s	
Lane Wavelength Range	Lane0	844		858	nm	
	Lane1	874		888		
	Lane2	904		918		

	Lane3	934		948		
Difference in launch power between any two lanes				4.5	dBm	
RMS Spectral width @850nm @880nm,910nm,940nm	Lane0 Lane1 Lane2 Lane3			 0.53 0.59	nm	
Optical Modulation Amplitude (OMA), each lane		-5.5		3	dBm	
Average Launch power per Lane		-7.5		3	dBm	
Launch Power Tx OMA-TDP	Lane0 Lane1 Lane2 Lane3	-6.4 -6.0 -6.5 -7.0			dBm	
Transmitter and Dispersion Eye Closure	Lane0 Lane1			3.7 4.0	dB	

	Lane2 Lane3			4.5 5.0		
Extinction Ratio		2			dB	
Optical Return Loss Tolerance		12			dB	
Average Launch Power per Lane @ TX Off State				-30	dBm	
Encircled Flux		>=86% at 19um <=30% at 4.5um				
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5x10-5 hits per sample		{0.23,0.34,0.43,0.27,0.35,0.4}				

Receiver Parameter	Lane	Min	Typical	Max	Unit	Note
Signaling rate, each lane		10.3125 , 9.953±100ppm			Gb/s	
Lane Wavelength Range	Lane0	844		858	nm	
	Lane1	874		888		

	Lane2	904		918		
	Lane3	934		948		
Damage threshold, each lane		3.8			dBm	
Average Receive Power, each lane		-12.9 -12.5 -12.2 -11.9		2.4	dBm	
Receiver Power, each lane (OMA)				3	dBm	
Receiver sensitivity OMA, per lane				-9.1	dB	
Difference in receive power between any two lanes(OMA)				5	dB	
RX_Los_Assert		-30			dBm	
RX_Los_De-ASSERT				-13	dBm	

RX_Los_Hysteresis		0.5			dBm	
Return reflectance				-12	dB	

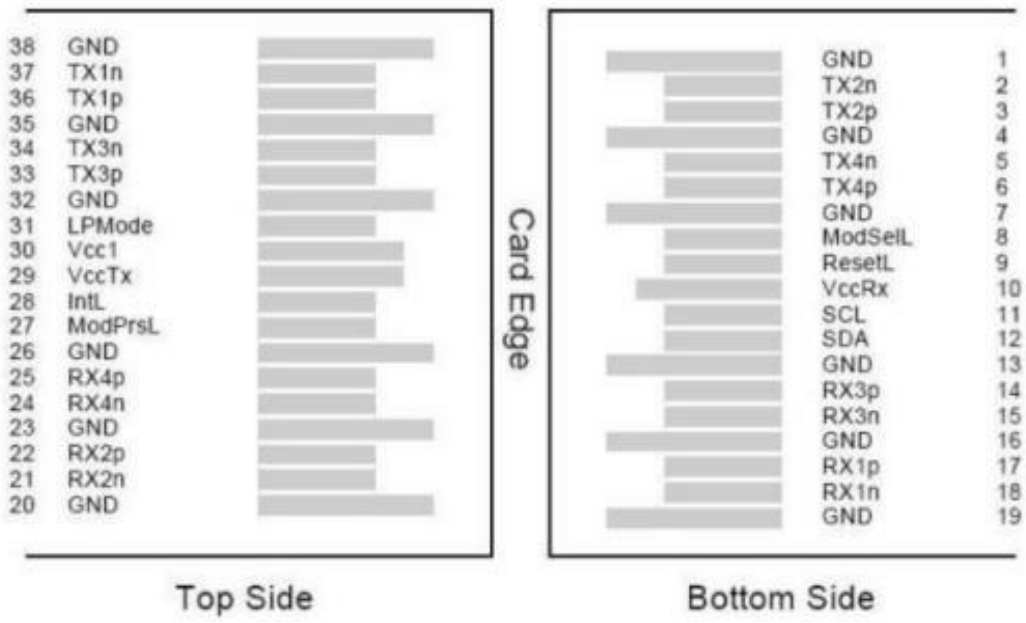
Digital Diagnostics

The following characteristics are defined over recommended operating conditions.

Parameter	Accuracy	Unit
Internally measured transceiver temperature	+/-3	° C
Internally measured transceiver supply voltage	+/-3	%
Measured Tx bias current	+/-10	%
Measured Tx output power	+/-3	dB
Measured Rx received average optical power	+/-3	dB

Pin Diagram

QSFP+ Transceiver Pad Layout, host PCB QSFP+ Pinout, and PIN Descriptions are as follows:



QSFP+ Transceiver Electrical Pad Pinout

Pin Definitions

Pin#	Name	Logic	Description	Power Seq.	Note
1	GND		Ground	1st	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3rd	
3	Tx2p	CML-I	Transmitter Non-Inverted Data output	3rd	
4	GND		Ground	1st	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3rd	
6	Tx4p	CML-I	Transmitter Non-Inverted Data output	3rd	
7	GND		Ground	1st	1
8	ModSelL	LVTLL-I	Module Select	3rd	
9	ResetL	LVTLL-I	Module Reset	3rd	
10	VccRx		+3.3V Power Supply Receiver	2nd	2
11	SCL	LVCMOS-I/O	2-Wire Serial Interface Clock	3rd	
12	SDA	LVCMOS-I/O	2-Wire Serial Interface Data	3rd	
13	GND		Ground	1st	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3rd	
15	Rx3n	CML-O	Receiver Inverted Data Output	3rd	
16	GND		Ground	1st	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3rd	
18	Rx1n	CML-O	Receiver Inverted Data Output	3rd	
19	GND		Ground	1st	1

20	GND		Ground	1st	1
21	Rx2n	CML-O	Receiver Inverted Data Output	3rd	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3rd	
23	GND		Ground	1st	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3rd	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	3rd	
26	GND		Ground	1st	1
27	ModPrsL	LVTTL-O	Module Present	3rd	
28	IntL	LVTTL-O	Interrupt	3rd	
29	VccTx		+3.3 V Power Supply transmitter	2nd	2
30	Vcc1		+3.3 V Power Supply	2nd	2
31	LPMode	LVTTL-I	Low Power Mode	3rd	
32	GND		Ground	1st	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3rd	
34	Tx3n	CML-I	Transmitter Inverted Data Output	3rd	
35	GND		Ground	1st	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3rd	
37	Tx1n	CML-I	Transmitter Inverted Data Output	3rd	
38	GND		Ground	1st	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP+ transceiver module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Recommended Interface Circuit

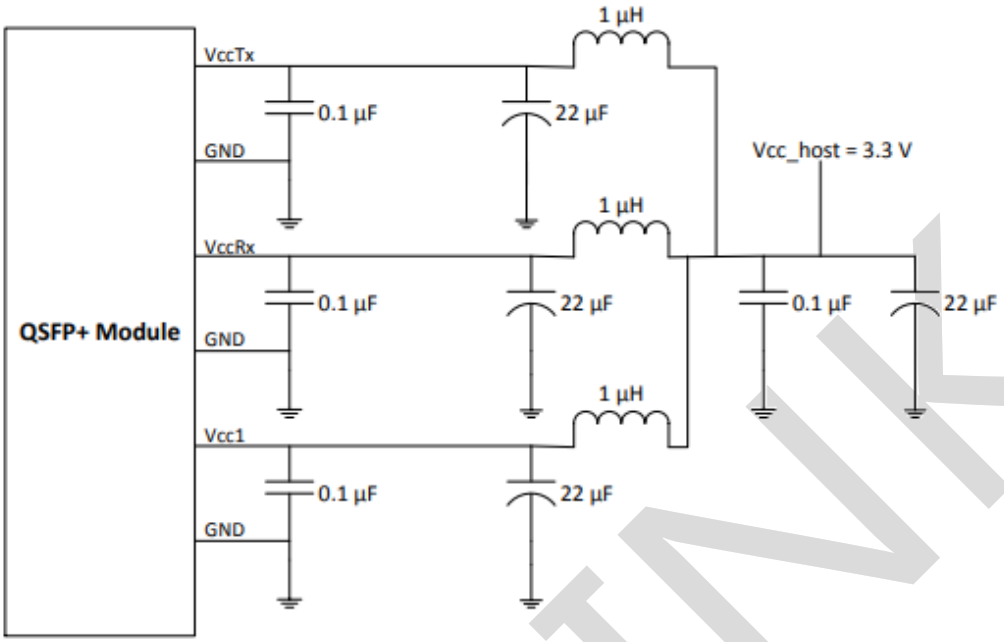
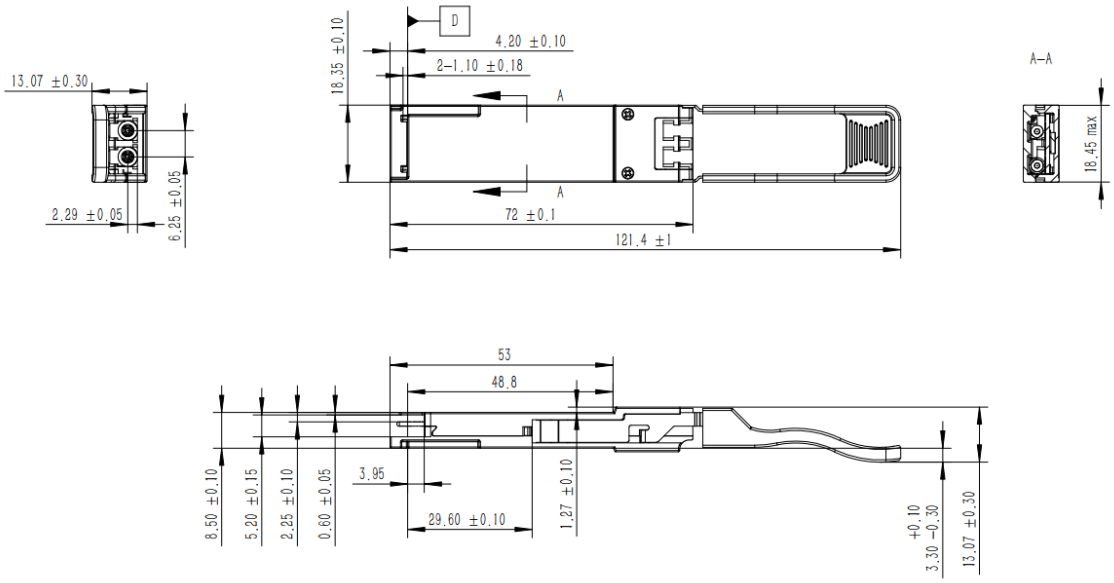


FIGURE 5-4 RECOMMENDED HOST BOARD POWER SUPPLY FILTERING

Mechanical Diagram

Figure shows the package dimensions of the module. The module is designed to becomplaint with QSFP+ MSA specification. Package dimensions are specified in SFF-8436.



Revision History

Version No.	Date	Description
1.0	February 18, 2019	Preliminary datasheet
2.0	July 15,2024	Format change

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