EQP400-DR4

400Gb/s QSFP112 500M DDM Transceiver

PRODUCT FEATURES

- Compliant to QSFP112 MSA Rev 2.0
- Parallel 4 Optical Lanes
- IEEE 802.3bs 400GBASE-DR4 Specification compliant
- Maximum power consumption 10W
- Compliant with IEEE Std 802.3ck, IEEE Std 802.3bs
- Compliant with 400Gbase-DR4 optical specifications
- Compliant with QSFP112 MSA Ver 2.0 type2
- Form factor of QSFP112 type2(87.4mm)
- Compliant with CMIS5.0 Management interface specifications
- MPO12 receptacle with APC end face
- 4x106. 25Gb/ selectrical interface (400GAUI-4)
- Up to 0.5km transmission on single mode fiber (SMF) with FEC
- Case temperature range: 0 ~ +70℃
- Maximum power consumption 10W
- RoHS 2.0 complaint

APPLICATIONS

- 400G Ethernet
- Data Center Interconnect
- Infiniband Interconnect
- Enterprise Networking

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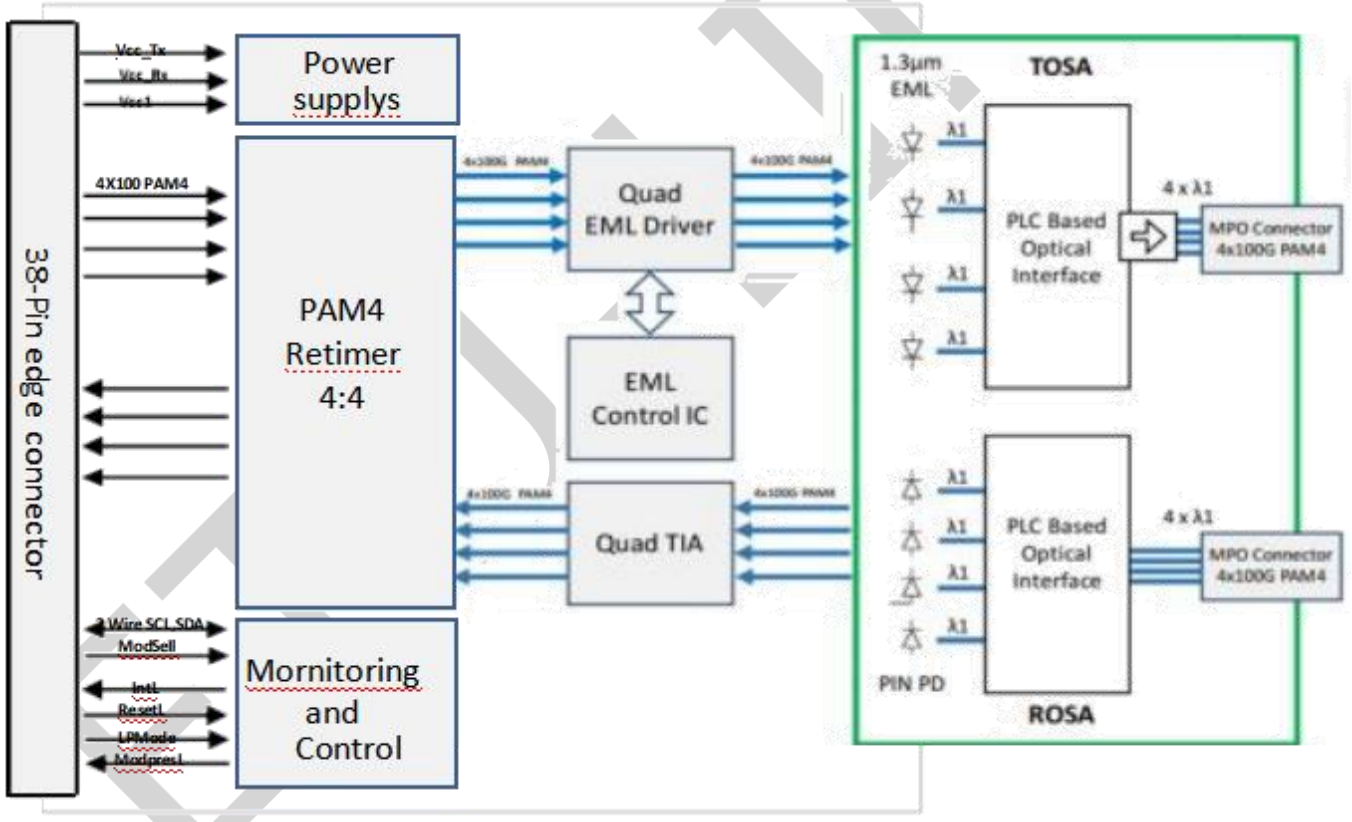
DESCRIPTIONS

This product is a 400Gb/s QSFP112 optical module designed for 0.5Km optical communication applications. The module converts 4 channels of 100Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s.

On the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 4 channels of 100Gb/s (PAM4) electrical output data.

An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP112 DR4 module receptacle. Host FEC is required to support up to 0.5Km fiber transmission.

Module Block Diagram



Ordering Information

Part Number	Description
EQP400-DR4	400G QSFP112 DR4 Optical Transceiver

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	TSTG	-40	+85	ºC
Supply Voltage	VCC	0	4	V
Relative Humidity	RH	10% to 90% non-condensing		

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Case Temperature- Operating	TCASE	0	70	ºC
Supply Voltage	Vcc	3.14	3.46	V
Power Consumption	PDISS		10	W
Pre-FEC Bit Error Ratio			$2.4x10^{-4}$	
Post-FEC Bit Error Ratio			$1x10^{-12}$	
Link Distance			500	M

Optical and Characteristics

Parameter	Min	Typical	Max	Unit	Note
Transmitter					
Signaling rate each lane		53.125		GBd	
Lane Wavelength Range	1304.5	1310	1317.5	nm	
Modulation Format	PAM4				
Average Optical Power per lane	-2.9		4	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane	-0.8		4.2	dBm	
Average Launch Power per Lane @ TX Off State			-15	dBm	
Launch Power in OMAouter minus TDECQ, each Lane	-2.2			dB	
Transmitter and Dispersion Eye Closure for PAM4, each Lane			3.4	dB	
Extinction Ratio	3.5			dB	
Relative Intensity Noise21.4 (OMA)			-136	dB/Hz	

Side-Mode Suppression Ration (SMSR)	30			dB	
Optical Return Loss Tolerance			21.4	dB	
Transmitter Reflectance			-26	dB	
Receiver					
Signaling rate each lane		53.125		GBd	
Lane Wavelength Range	1304.5	1310	1317.5	nm	
Modulation Format	PAM4				
Damage Threshold	5			dBm	
Average Receive Power, each lane	-5.9		4	dBm	
Receiver Power, each lane (OMA)			4.2	dBm	
Receiver Reflectance			-26	dB	
Receiver Sensitivity each lane (OMA_{outer})			Equation	dBm	1
Stressed Receiver Sensitivity (OMAouter), each			-1.9	dBm	
Stressed Conditions for Stress Receiver Sensitivity					
Stressed Eye Closure for PAM4 (SECQ),Lane under Test		3.4		dB	
OMAouter of each Aggressor Lane		4.2		dBm	

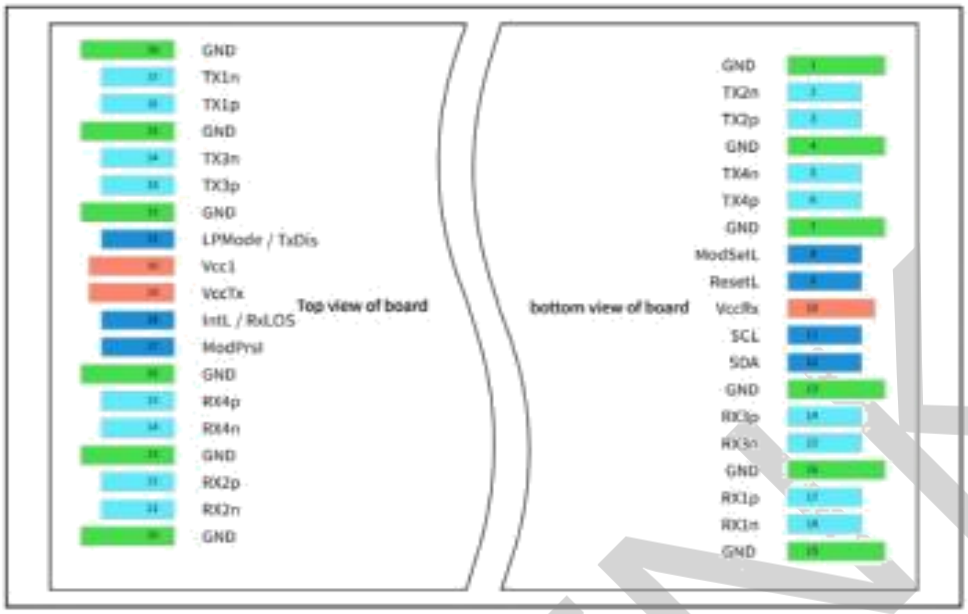
Notes:

1. 1.Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. It should meet Equation: RS=max (-3.9, -SECQ5.3), where RS is the receiver sensitivity, and SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

Digital Diagnostics

Parameters	Unit	Specification
Temperature Monitor absolute error	◦ C	±3
Supply Voltage Monitor absolute error	%	±5
I_bias Monitor absolute error	%	±10
Received Power (Rx) Monitor absolute error	dB	±3.0
Transmit Power (Tx) Monitor absolute error	dB	±3.0

Pin Diagram



Pin Definitions

Pin No.	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	TX2n	Transmitted Inverted Data Input	3	
3	CML-I	TX2p	Transmitted Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	TX4n	Transmitted Inverted Data Input	3	
6	CML-I	TX4p	Transmitted Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSeil	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3 VDC Receiver Power Supply	2	2
11	LVCMOS-I/O	SCL	Serial Clock for I2C Interface	3	
12	LVCMOS-I/O	SDA	Serial Data for I2C Interface	3	
13		GND	Ground	1	1
14	CML-O	RX3p	Receiver Non-Inverted Data Output	3	
15	CML-O	RX3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	RX1p	Receiver Non-Inverted Data Output	3	
18	CML-O	RX1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1

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20		GND	Ground	1	1
21	CML-O	RX2n	Receiver Inverted Data Output	3	
22	CML-O	RX2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	RX4n	Receiver Inverted Data Output	3	
25	CML-O	RX4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	3	
29		Vcc Tx	+3.3 VDC Transmitter Power Supply	2	2
30		Vcc1	+3.3 VDC Power Supply	2	2
31	LVTTL-I	LPMode/Tx dis	Low Power Mode/optioanl Tx Disable	3	
32		GND	Ground	1	1
33	CML-I	TX3p	Transmitted Non-Inverted Data Input	3	
34	CML-I	TX3n	Transmitted Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	TX1p	Transmitted Non-Inverted Data Input	3	
37	CML-I	TX1n	Transmitted Inverted Data Input	3	
38		GND	Ground	1	1

2. Note 1: GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
3. Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements, defined for the host side of the Host Edge Card Connector, are listed in Table 4. Recommended
4. host board power supply filtering is shown in Figure 4. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

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Recommended Interface Circuit

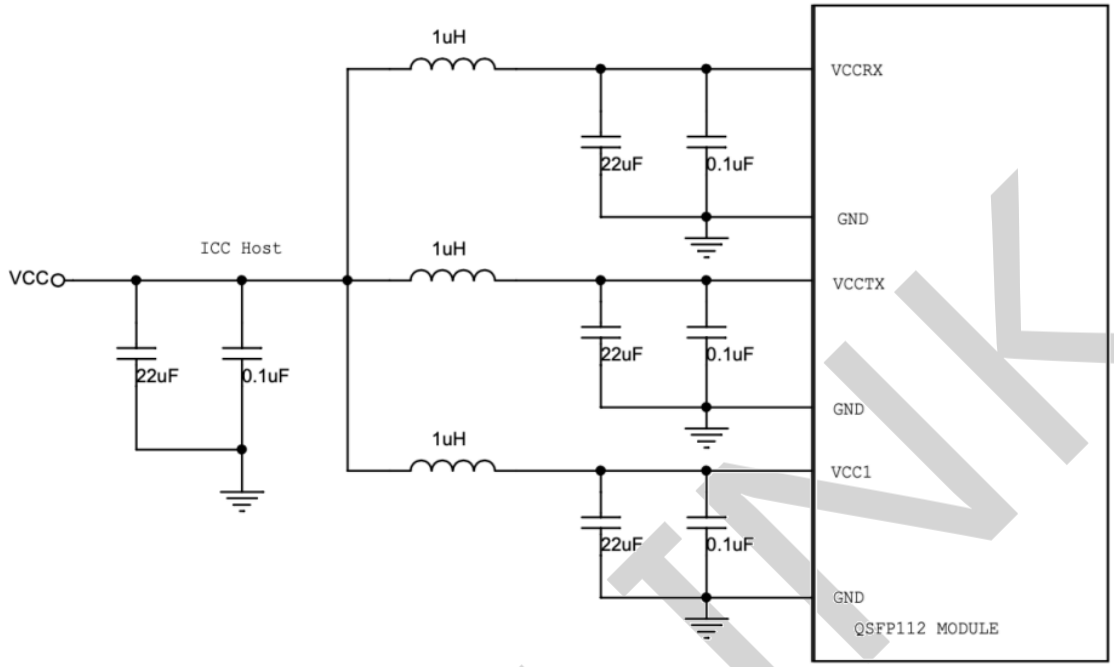
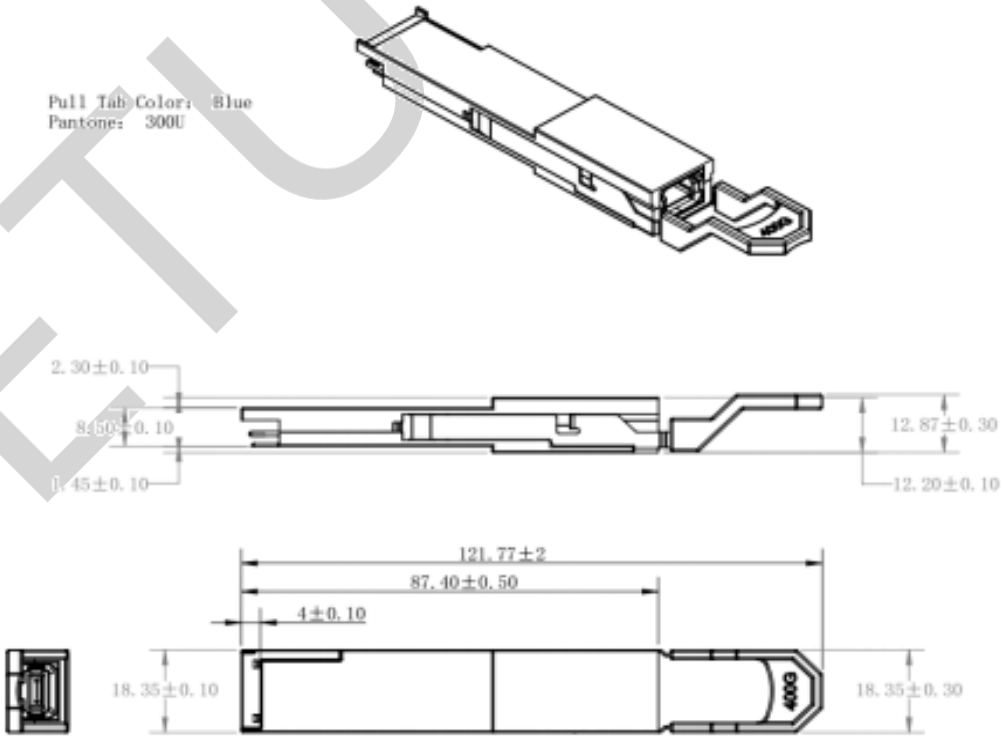


Figure 7 Recommended host board power supply filtering

Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	February 18, 2023	Preliminary datasheet
2.0	August 05,2024	Format change

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