EQD400-LR4

400G QSFP-DD LR4 Optical Transceiver

Product Features

- Compliant with QSFP-DD MSA
- Compliant with 100G Lambda MSA 400G-LR4 Specification compliant
- Compliant with CMIS5.0
- Compliant with IEEE Std 802.3bs
- 8x53. 125Gb/s electrical interface (400GAUI-8)
- Cooled EML laser with CWDM wavelength
- Up to 10km transmission on single mode fiber (SMF) with FEC
- Single +3.3V power supply
- Case temperature range: 0 ~ +70□
- Maximum power consumption 12W
- Duplex LC connector
- RoHS complaint

Applications

- 400G BASE-LR4 Ethernet
- Data Center Interconnect •Enterprise Networking

Description

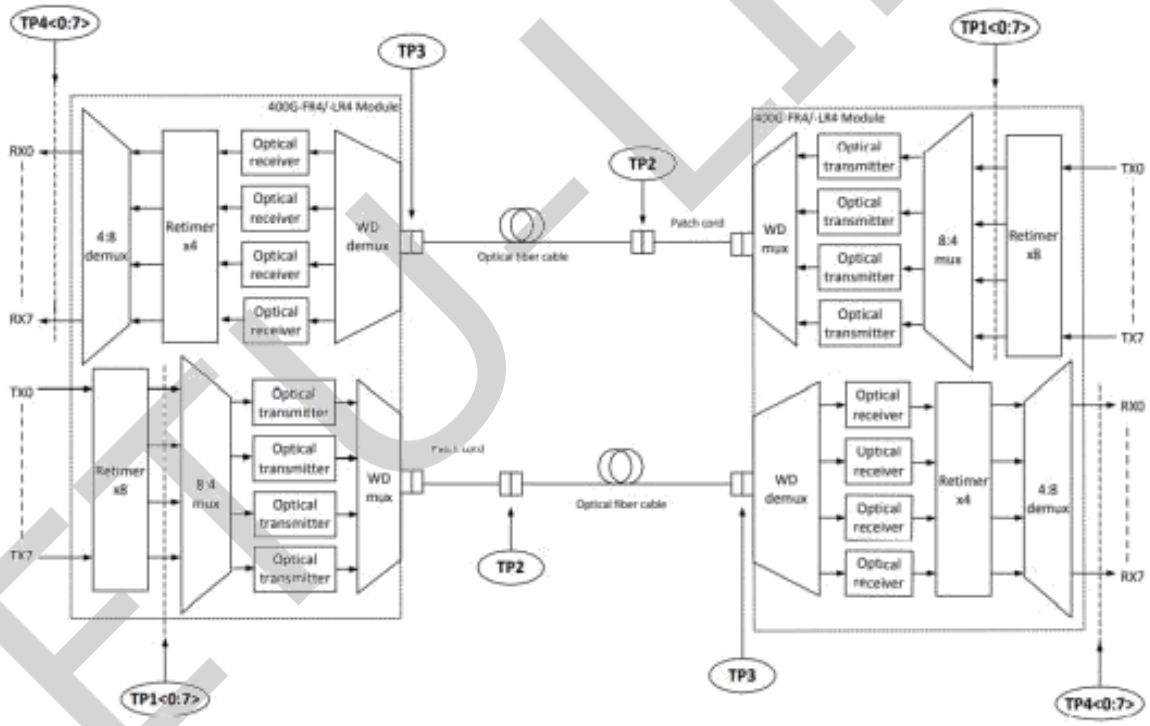
This product is a 400Gb/s QSFP-DD optical module designed for 10km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals and multiplexes them into a single channel for 400Gb/s optical transmission.

On the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals and converts them to 8 channels of 50Gb/s (PAM4) electrical output data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2.

Host FEC is required to support up to 10km fiber transmission.

Module Block Diagram



Ordering Information

Part Number	Description
EQD400-LR4	400G QSFP-DD LR4 Optical Transceiver

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	T_{STG}	-40	+85	ºC
Supply Voltage	V_{CC}	0	4	V
Relative Humidity	RH	10% to 90% non-condensing		

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Case Temperature- Operating	T_{CASE}	0	70	ºC
Supply Voltage	Vcc	3.14	3.46	V
Power Consumption	P_{DISS}		12	W
Pre-FEC Bit Error Ratio			$2.4x10^{-4}$	
Link Distance	2		10,	KM

Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Notes
Receiver electrical output characteristics at TP4					
Signaling rate per lane		26.5625		GBd	
AC common-mode output voltage(RMS)		-	17.5	mV	
Differential peak-to-peak output voltage			900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265		UI	
Near-end Eye height, differential	70			mV	
Near-end vertical eye closure			7.5	dB	
Far-end ESMW (Eye symmetry mask width)		0.20		UI	
Far-end Eye height, differential	30			mV	
Far-end vertical eye closure			7.5	dB	
Far-end pre-cursor ISI ratio	-4.5		2.5	%	
Common mode to differential conversion return loss	802.3 Equation(83E-3)			dB	
Differential output return loss	802.3 Equation(83E-2)			dB	
Differential termination mismatch			10	%	

Transition time (min, 20% to 80%)		9.5		ps	
DC common mode voltage	-350		2850	mV	
Transmitter electrical input characteristics at TP1					
Signaling rate, per lane		26.5625		GBd	
Differential peak-to-peak input voltage tolerance	900			mV	
Differential input return loss	802.3 Equation(83E-5)				
Differential to common mode input return loss	802.3 Equation(83E-6)			mV	
AC common-mode output voltage(RMS)			17.5	mV	
Single-ended voltage tolerance range	-0.4		3.3	V	
Module stressed input	802.3 120E.3.4.1			UI	
Differential termination mismatch			10	%	
DC common mode voltage	-350			mV	

Optical Characteristics

Transmitter Parameter	Lane	Min	Typical	Max	Units
Lane Wavelength Range	Lane 0	1264.5	1271	1277.5	nm
	Lane 1	1284.5	1291	1297.5	nm
	Lane 2	1304.5	1311	1317.5	nm
	Lane 3	1324.5	1331	1337.5	nm
Signal rate per lane			53.125		GBd
Average launch Power per lane		-2.7		5.1	dBm
Total Average launch power				11.1	dBm
Outer Optical Modulation Amplitude (OMAouter), each lane for TDECQ<1.4 dB for 1.4dB<=TDECQ<=3.9dB		0.3 -1.1+TDECQ		4.4	dBm
Difference in launch power between any two lanes (OMAouter)				4	dB
Average Launch Power per Lane @ TX Off State				-16	dBm
Transmitter Eye Closure for PAM4(TECQ),each Lane				3.9	dB
Transmitter and dispersion Eye Closure for PAM4(TDECQ), each Lane				3.9	dB
|TDECQ - TECQ|				2.5	dB
Extinction Ratio		3.5			dB
Relative Intensity Noise (OMA)				-136	dB/H

					z
Side-Mode Suppression Ration (SMSR)		30			dB
Optical Return Loss Tolerance				15.6	dB
Transmitter Reflectance				-26	dB
Transmitter over/under-shoot				25	%
Transmitter peak-to-peak power				5.2	dBm
Transmitter transition time				17	ps

Receiver Optical Specifications

Receiver Parameter	Lane	Min	Typical	Max	Units
Lane Wavelength Range	Lane 0	1264.5	1271	1277.5	nm
	Lane 1	1284.5	1291	1297.5	nm
	Lane 2	1304.5	1311	1317.5	nm
	Lane 3	1324.5	1331	1337.5	nm
Signal rate per lane			53.125		GBd
Damage Threshold		6.1			dBm
Average Receive Power, each lane		-9		5.1	dBm
Receiver Power, each lane (OMA)				4.4	dBm
Receiver Reflectance				-26	dB
Difference in receive Power between any Two Lanes(OMAouter)				4.3	dBm
Receiver Sensitivity each lane (OMAouter) for TECQ<1.4dB for 1.4dB<=TECQ<=3.9dB				-6.8 - 8.2+TECQ	dBm
Stressed Receiver Sensitivity (OMAouter), each				-4.3	dBm
Stressed Conditions for Stress Receiver Sensitivity					
Stressed Eye Closure for PAM4 (SECQ),Lane under Test			3.9		dB
OMAouter of each Aggressor Lane			-0.4		dBm

Receiver Output Power Thresholds for Loss of Signal(LOS)

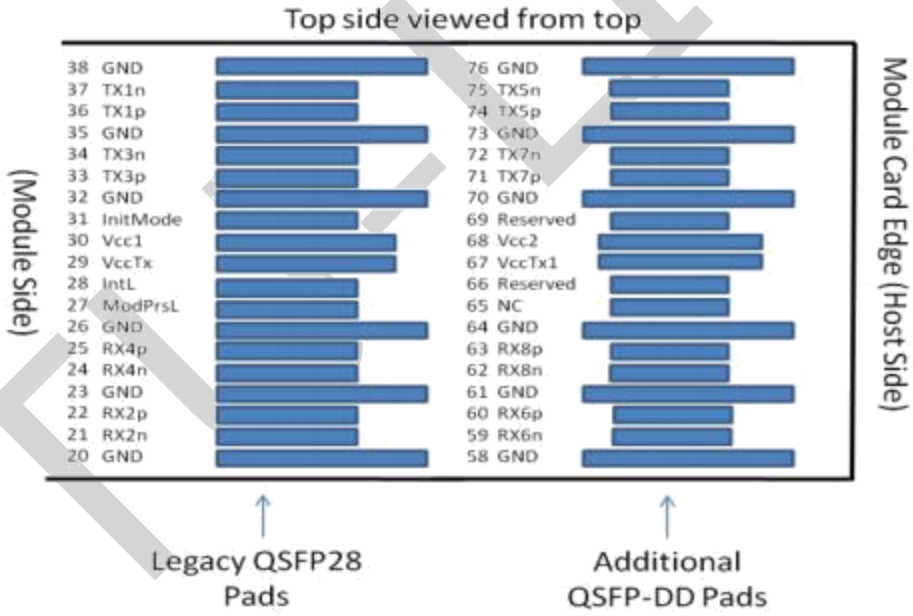
Parameter	Min	Typical	Max	Unit
RX_LOS_Assert Min/Max	-20.0			dBm

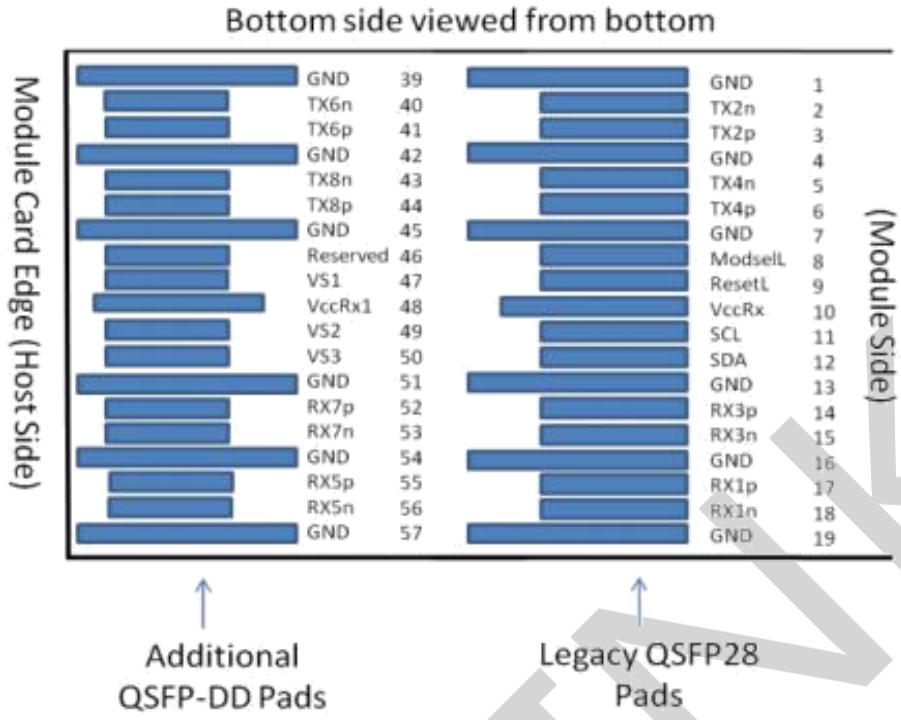
RX_LOS_De-Assert Min/Max			-12.2	dBm
RX_LOS_Hysteresis	0.5			dB

Digital Diagnostic Functions

Parameters	Unit	Specification
Temperature Monitor absolute error	。C	±3
Supply Voltage Monitor absolute error	%	±5
I_bias Monitor absolute error	%	±10
Received Power (Rx) Monitor absolute error	dB	±3.0
Transmit Power (Tx) Monitor absolute error	dB	±3.0

Pin Definition





PIN Description

Pin No.	Symbol	Description	Note
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	

19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	Init Mode	Initialization mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data output	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data output	
45	GND	Ground	1
46	Reserved	For Future Use	3
47	VS1	Module Vendor Specific 1	3
48	VccRx1	3.3V Power Supply	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	

53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For Future Use	3
67	VccTx1	3.3V power supply	2
68	Vcc2	3.3V power supply	2
69	Reserved	For Future Use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Output	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Output	
76	GND	Ground	1

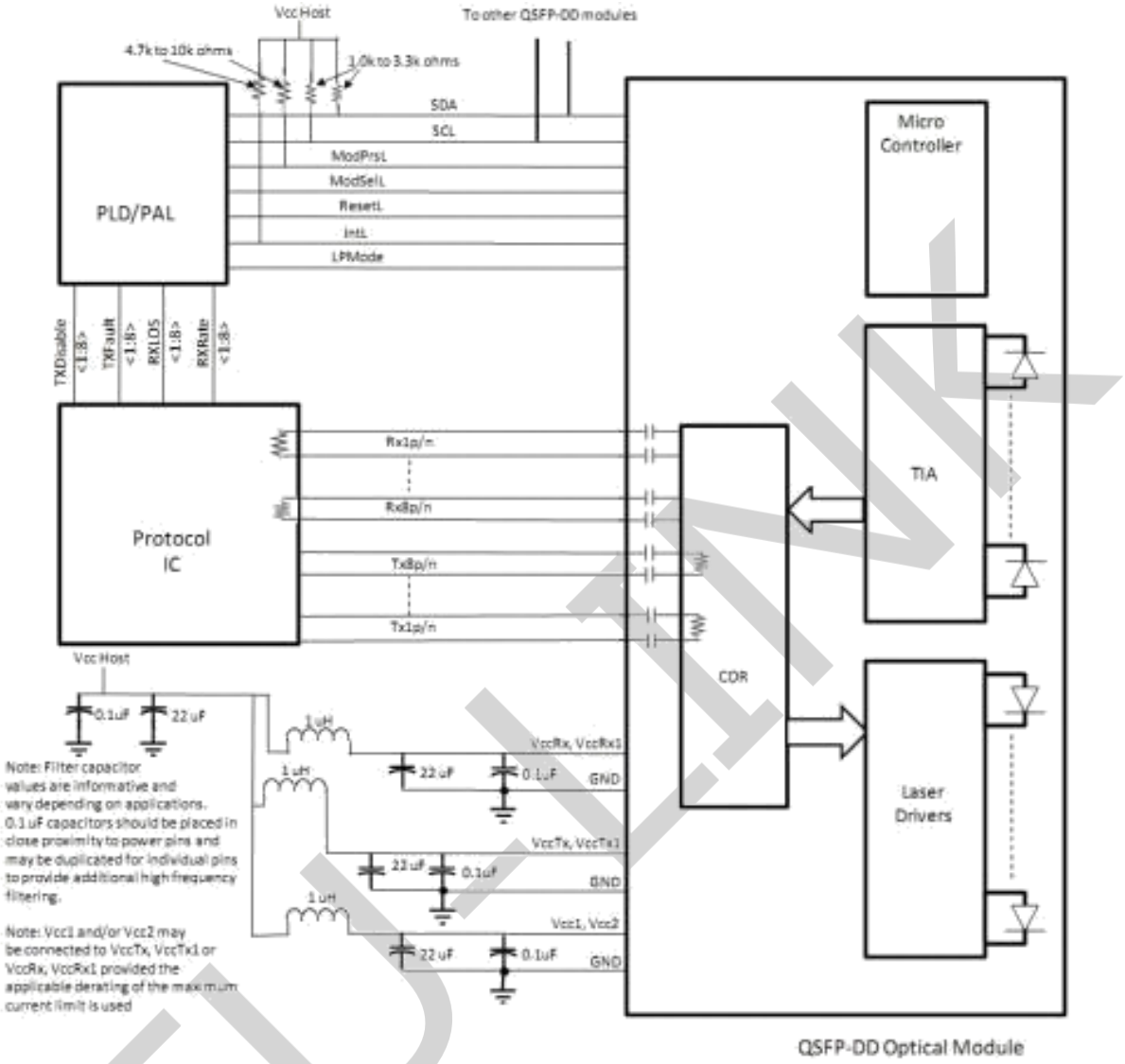
Note:

1．QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

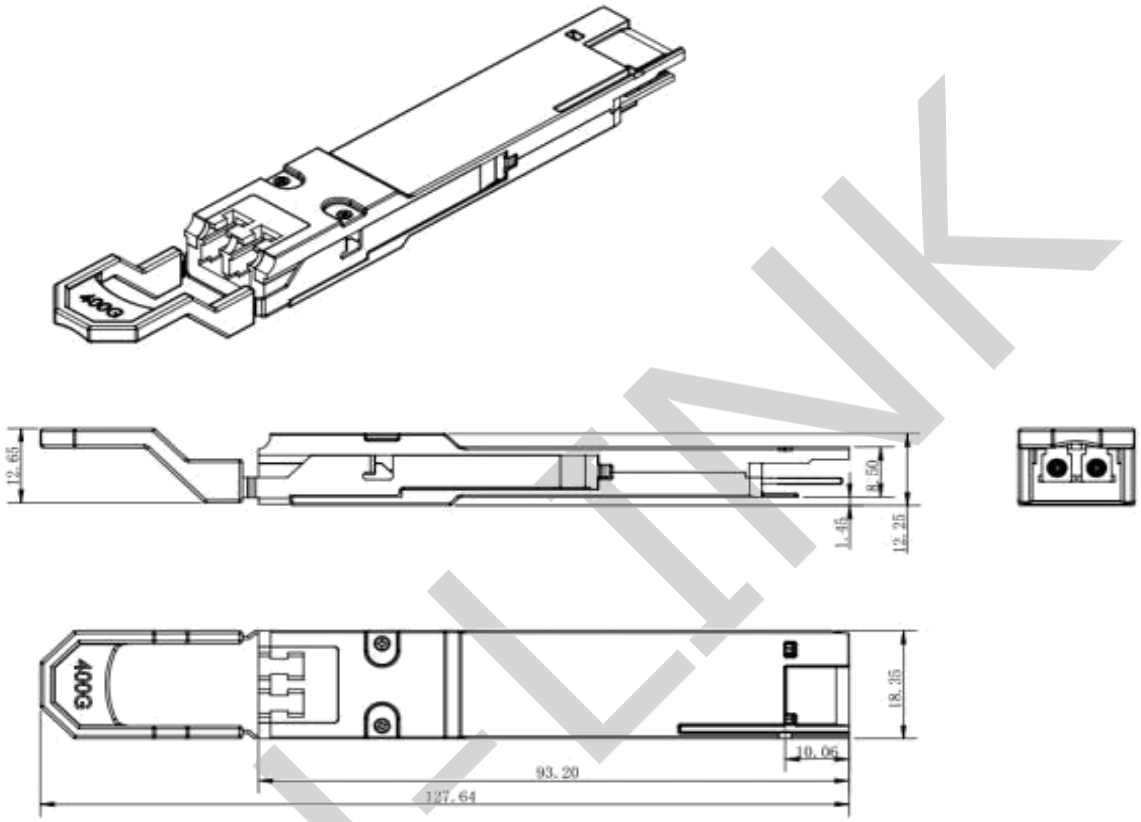
2．VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 8. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. For power classes 4 and above the module differential loading of input voltage pins must not result in exceeding pin current limits. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3． All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 □ to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 k and less than 100 pF.

Recommended application circuit



Mechanical Dimensions



Revision History

Version No.	Date	Description
1.0	February 18, 2022	Preliminary datasheet
2.0	July 13,2024	Format change

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