

EOP400-SR4

OSFP112 400G SR4 Optical transceiver for (dual MPO) flat top solution

PRODUCT FEATURES

- Up to 106.25 Gbps data rate per channel by PAM4 modulation
- Support 400GAUI-4 electrical interface
- Integrated 850nm VCSEL array and PD array
- DDM function implemented
- Hot-pluggable
- Single +3.3V power supply
- Compliant to OSFP MSA 5.0
- Compliant with CMIS 4.0
- 4x106.25Gb/s electrical interface (400GAUI-4)
- Maximum power consumption 9W
- Single +3.3V power supply
- Case temperature range: 0 ~ +70°C
- RoHS 2.0 complaint

APPLICATIONS

- Data centers and Cloud Networks

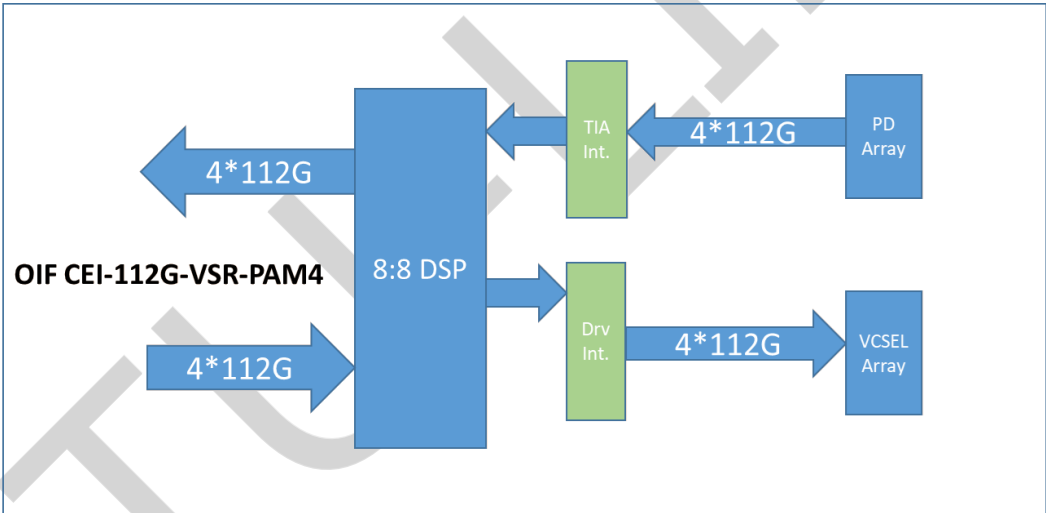
DESCRIPTIONS

This product is a 400Gb/s OSFP112 400G SR4 optical module designed for 100m optical communication applications. The module converts 4 channels of 100Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s.

On the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 4 channels of 100Gb/s (PAM4) electrical output data.

An optical fiber cable with an single MPO-12 connector can be plugged into the OSFP112 400G SR4 module receptacle. Host FEC is required to support up to 100m fiber transmission.

Module Block Diagram



Ordering Information

Part No.	Data Rate(optical)
EOP400-SR4	OSFP112 400G SR4 Optical transceiver for flat top solution

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
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Storage Temperature Range	TSTG	-40	+85	°C
Supply Voltage	VCC	-0.5	3.6	V
Relative Humidity	RH	5% to 95%		
		non-condensing		

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Case Temperature- Operating	TCASE	0	70	°C
Supply Voltage	Vcc	3.135	3.465	V
Power Consumption	PDISS		9	W
Pre-FEC Bit Error Ratio			2.4x10 ⁻⁴	
Link Distance over OM3		0.5	30	M
Link Distance over OM4		0.5	50	M

Electrical and Optical Characteristics

Transmitter Parameter	Min	Typical	Max	Unit
Signaling rate each lane	53.125±100ppm			GBd
Lane Wavelength Range		850		nm
RMS Spectral width			0.6	nm
Modulation Format	PAM4			
Average Optical Power per lane	-4.6		4	dBm
Outer Optical Modulation Amplitude (OMA _{outer}), each lane for TDECQ≤1.8dB	-2.6		3.5	dBm
for 1.8<TDECQ≤4.4dB	-4.4+TDECQ		3.5	
Outer Optical Modulation Amplitude (OMA _{outer}), each lane for TECQ≤1.8dB	-2.6		3.5	dBm
for 1.8<TECQ≤4.4dB	-4.4+TECQ		3.5	
Transmitter and Dispersion Eye Closure for PAM4, each Lane			4.4	dB
Transmitter Eye Closure for PAM4(TECQ), each Lane			4.4	dB
Extinction Ratio	2.5			dB
Transmitter excursion ,each lane			2	dB
Transmitter transition time,each lane			17	ps
Average Launch Power per Lane @ TX Off State			-30	dBm
Relative Intensity Noise ₁₂ (OMA)			-131	dB/Hz
Optical Return Loss Tolerance			12	dB
Encircled Flux	≥86% at 19um ≤30% at 4.5um			dB

Receiver Parameter				
Signaling rate each lane	53.125±100ppm			GBd
Lane Wavelength Range	850			nm
Modulation Format	PAM4			
Damage Threshold	5			dBm
Average Receive Power, each lane	-6.4		4	dBm
Receiver Power, each lane (OMA)			3.5	dBm
Receiver Sensitivity each lane (OMAouter) for TECQ≤1.8dB for 1.8<TECQ≤4.4dB			-4.6 -6.4+TECQ	dBm
Receiver reflectance			-12	dB
Stressed Receiver Sensitivity (OMAouter), each			-2	dBm
Stressed Conditions for Stress Receiver Sensitivity				
Stressed Eye Closure for PAM4 (SECQ), Lane under Test		4.4		dB
OMAouter of each Aggressor Lane		3.5		dBm
RX_LOS_Assert Min/Max	-15.0			dBm
RX_LOS_De-Assert Min/Max			-8.9	dBm
RX_LOS_Hysteresis		1.5		dB

Low Speed Electrical signal

Parameter	Symbol	Min	Max	Units	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for fast mode, 20mA for Fast-mode plus
	VOH	V _{CC} -0.5	V _{CC} +0.3	V	
SCL and SDA	VIL	-0.3	V _{CC} *0.3	V	
	VIH	V _{CC} *0.7	V _{CC} +0.5	V	
Capacitance for SCL and SDA I/O pin	C _i		14	pF	
Total bus capacitive load for SCL and SDA	C _b		100	pF	3.0k Ohms Pull up resistor, max
			200	pF	1.6k Ohms Pull up resistor, max
LPMODE/TxDis, Reset and ModeSelL	VIL	-0.3	0.8	V	I _{in} ≤ 125uA for V _{in} < V _{CC}
	VIH	2	V _{CC} + 0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0mA
	VOH	V _{CC} - 0.5	V _{CC} + 0.3	V	10k ohms pull-up to Host V _{CC}
ModPrsL	VOL	0	0.4	%	IOL=2.0mA
	VOH			dB	ModPrsL can be implemented as a short-circuit to GND on the module

High Speed Electrical signal

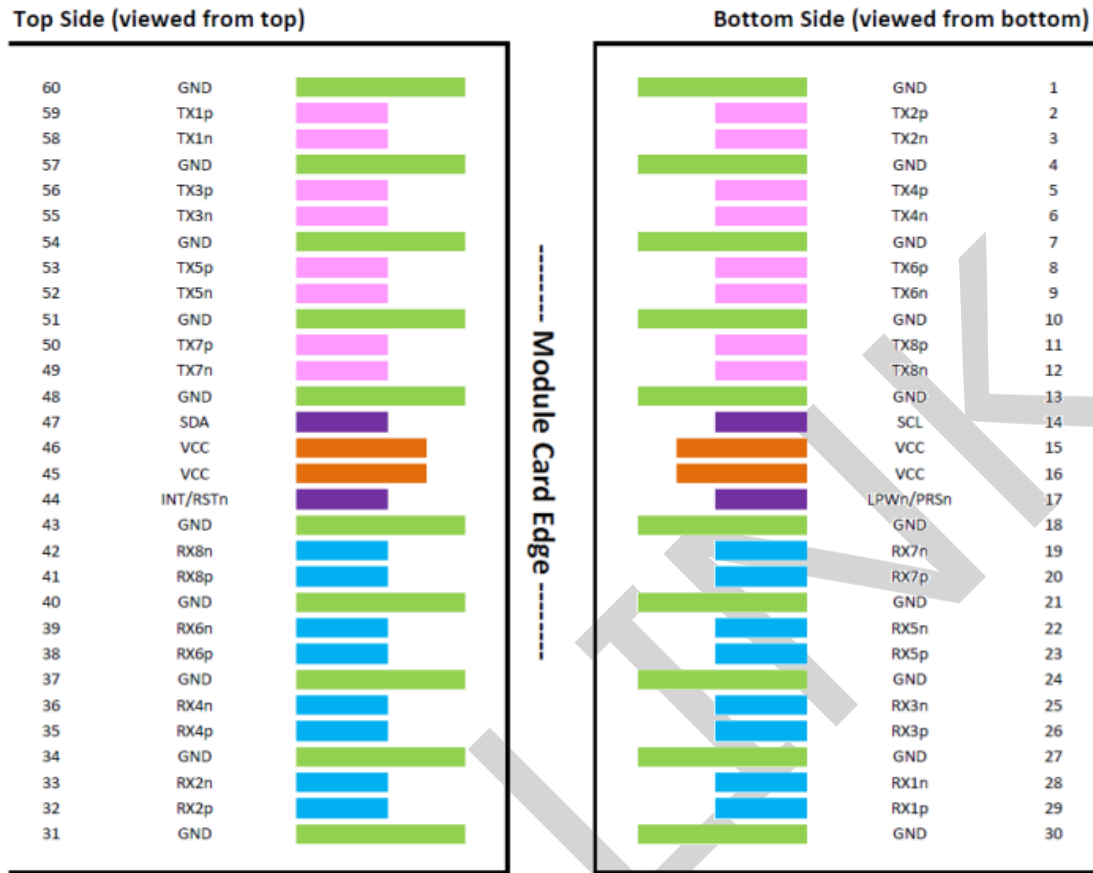
Parameter	Min	Typical	Max	Unit	Notes
Receiver electrical output characteristics at TP4					

Signaling rate per lane		53.125		GB	
AC common-mode output voltage(RMS)		-	17.5	mV	
Differential peak-to-peak output voltage			900	mV	
Near-end ESMW (Eye symmetry mask width)		TBD		UI	
Near-end Eye height, differential	24			mV	
Near-end vertical eye closure			7.5	dB	
Far-end ESMW (Eye symmetry mask width)		TBD		UI	
Far-end Eye height, differential	24			mV	
Far-end vertical eye closure			7.5	dB	
Far-end pre-cursor ISI ratio		TBD		%	
Common mode to differential conversion return loss	802.3ck 120G-1			dB	
Effective return loss	TBD			dB	
Differential termination mismatch			10	%	
Transition time (min, 20% to 80%)		TBD		ps	
DC common mode voltage	-350		2850	mV	
Transmitter electrical input characteristics at TP1					
Signaling rate, per lane		53.125		GB	
Differential pk-pk input voltage tolerance	900			mV	
Common-mode to differential return loss	802.3ck Equation(120G-1)				
Effective return loss	TBD				
Differential termination mismatch			10	%	
Module stressed input test	See 120G.3.4.1				
Single-ended voltage tolerance range	-0.4		3.3	V	
DC common-mode voltage	-350		2850	mV	

Digital Diagnostics

Parameters	Unit	Specification
Temperature Monitor absolute error	°C	± 3
Supply Voltage Monitor absolute error	%	± 5
I_bias Monitor absolute error	%	± 10
Received Power (Rx) Monitor absolute error	dB	± 3.0
Transmit Power (Tx) Monitor absolute error	dB	± 3.0

Pin Diagram



Note:

For OSFP112 400G SR4 end, Only CH1~CH4 available. CH5~CH8 not connect, TX5~8p/n,RX5~8p/n not connect.

Pin Definitions

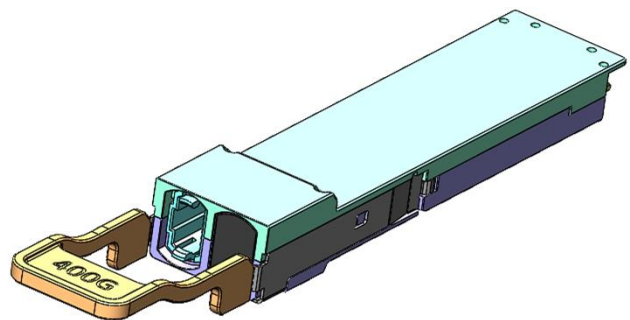
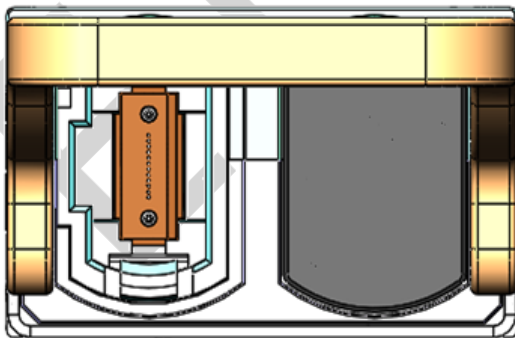
Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1

11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVC MOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1

44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVC MOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

Optical interface

The MPO-12 connectors for OSFP112 400G SR4.



Recommended Interface Circuit

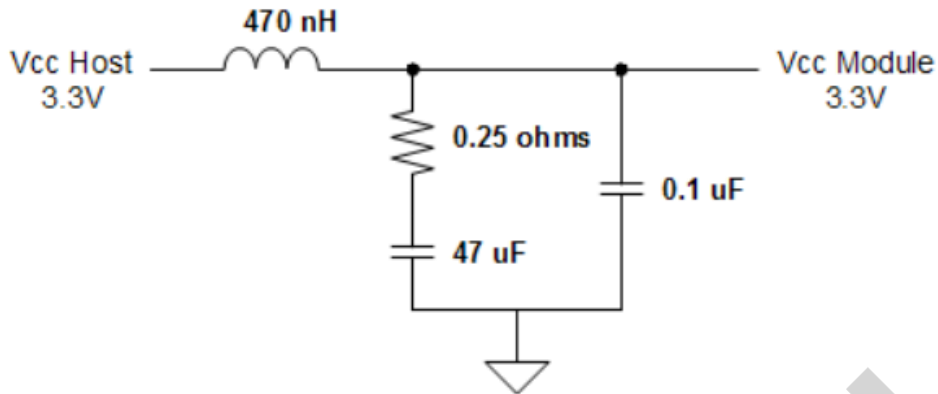
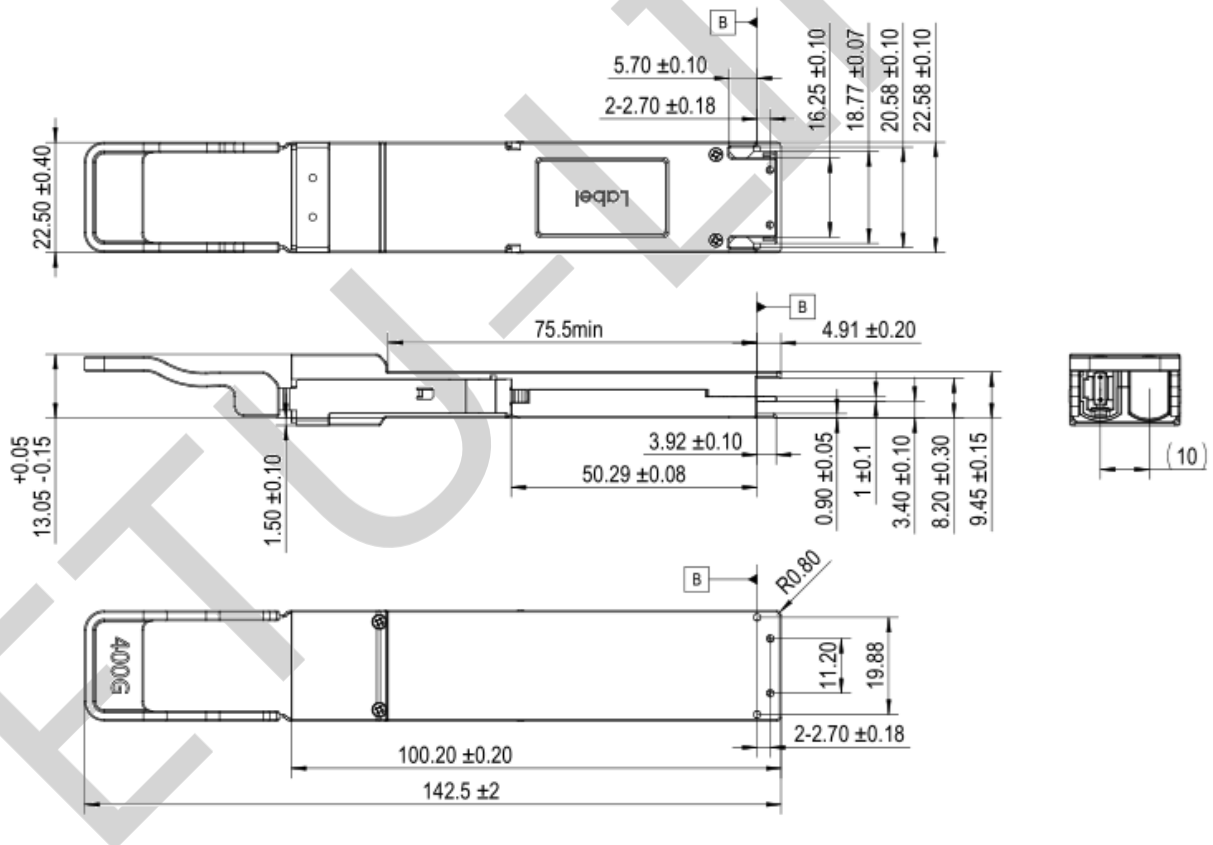


Figure 13-6: Host board power filter circuit

Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	February 18, 2024	Preliminary datasheet
1.1	Oct 05, 2024	Format change

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